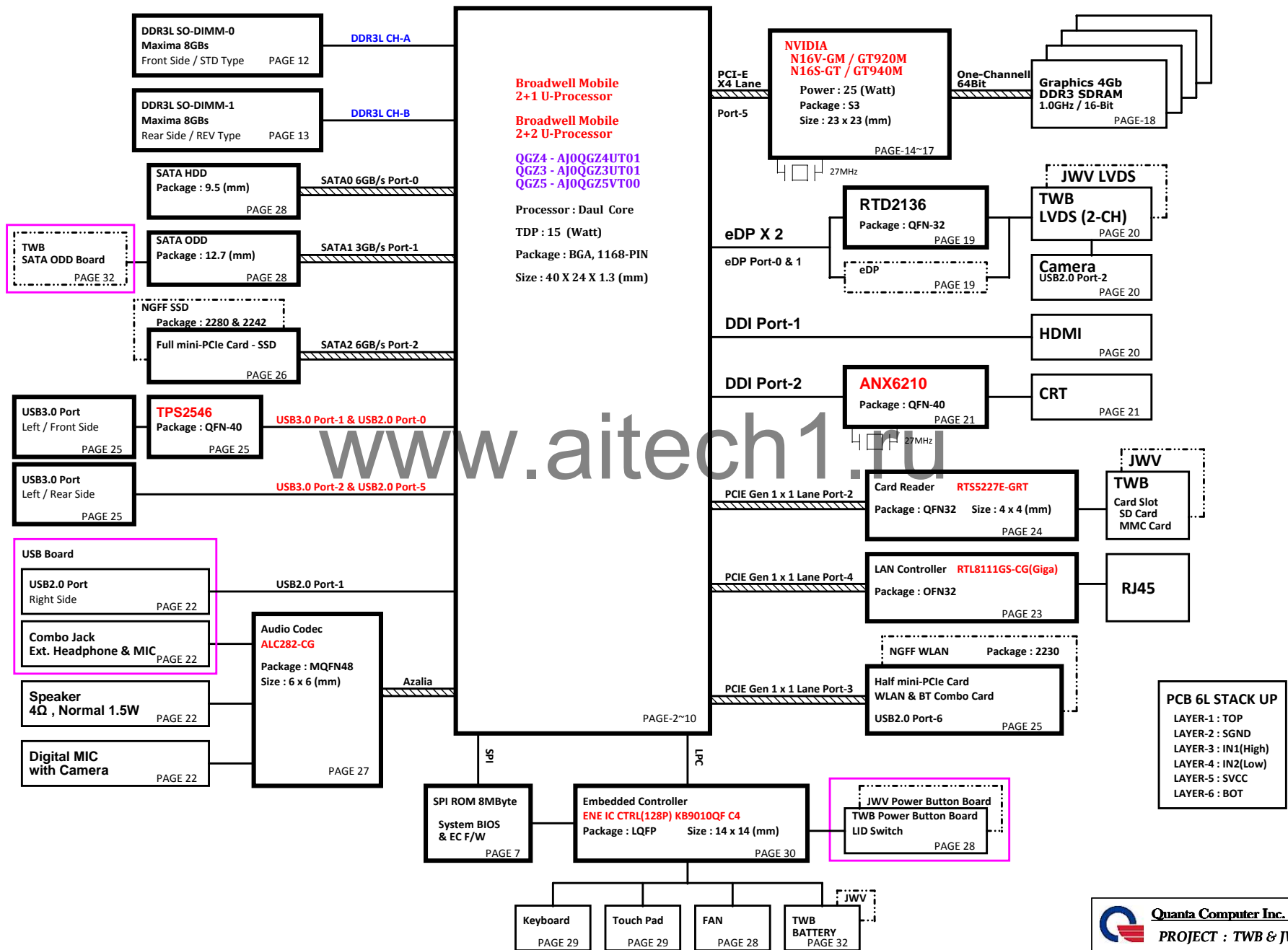
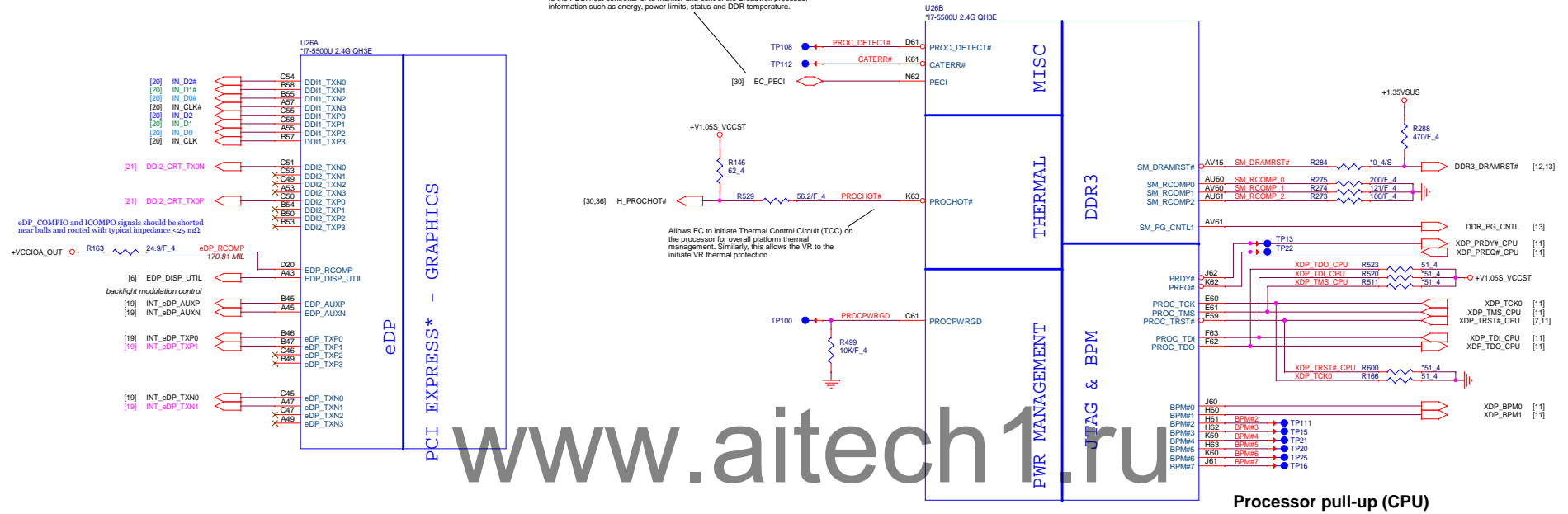


TWB + JWV Intel Boardwell ULT Platform Block Diagram

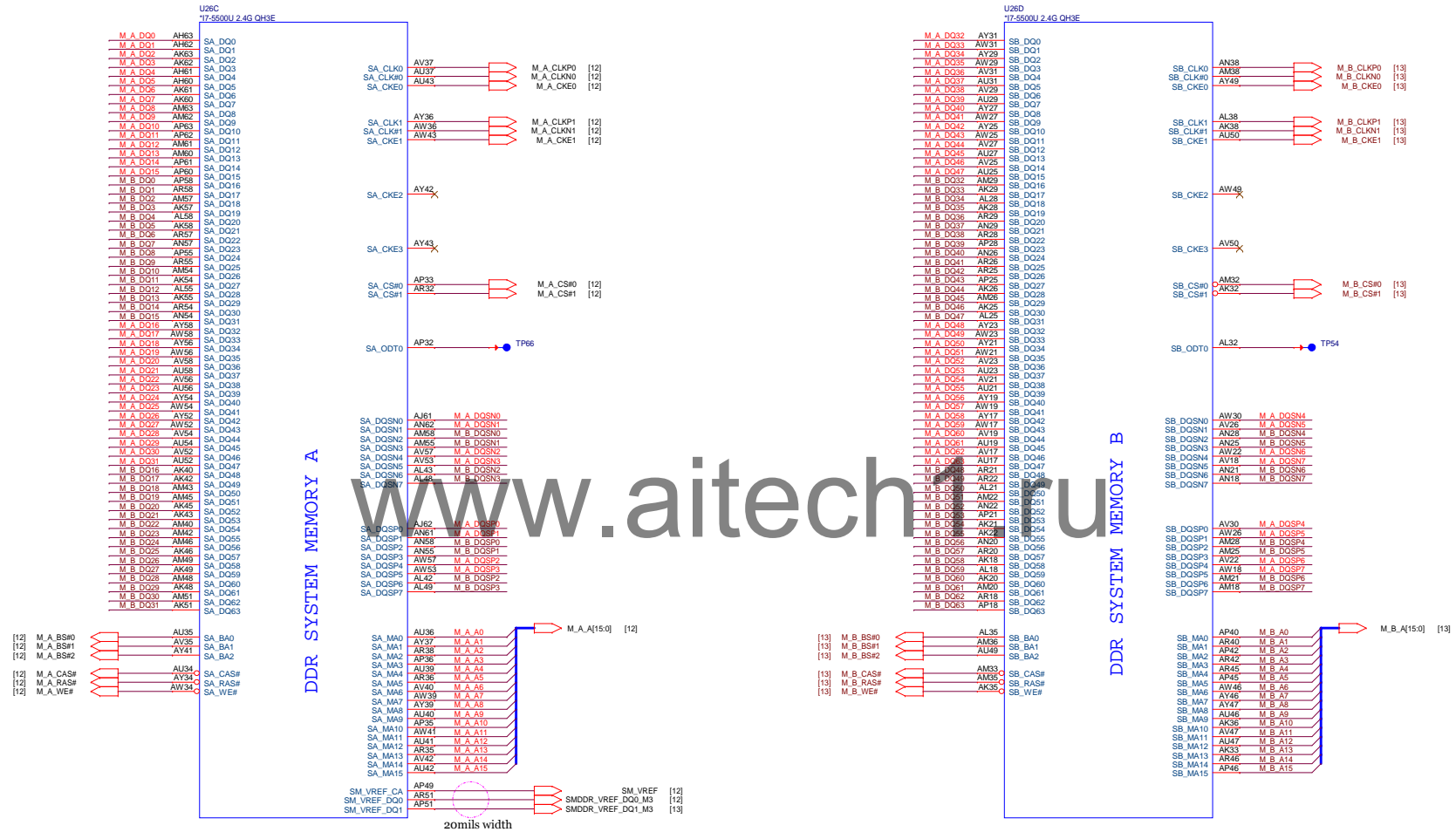


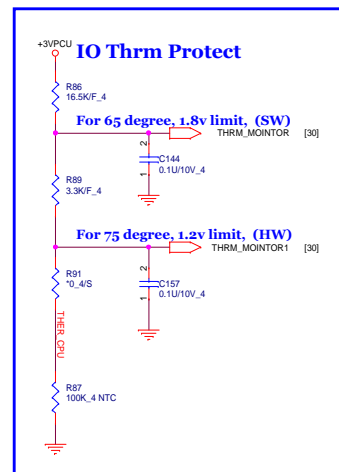
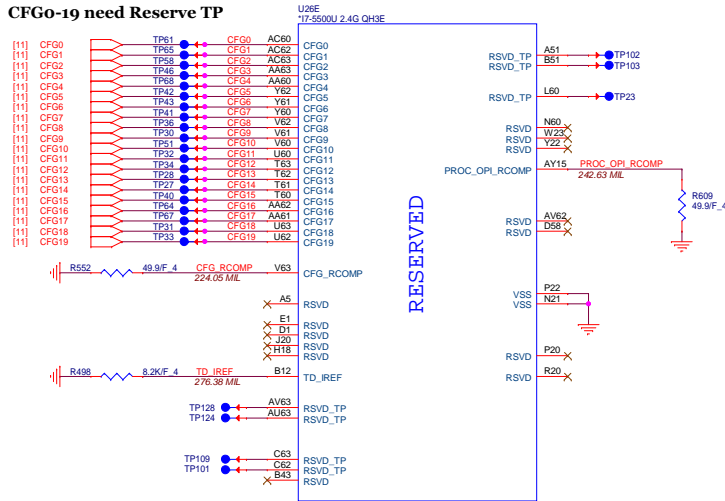
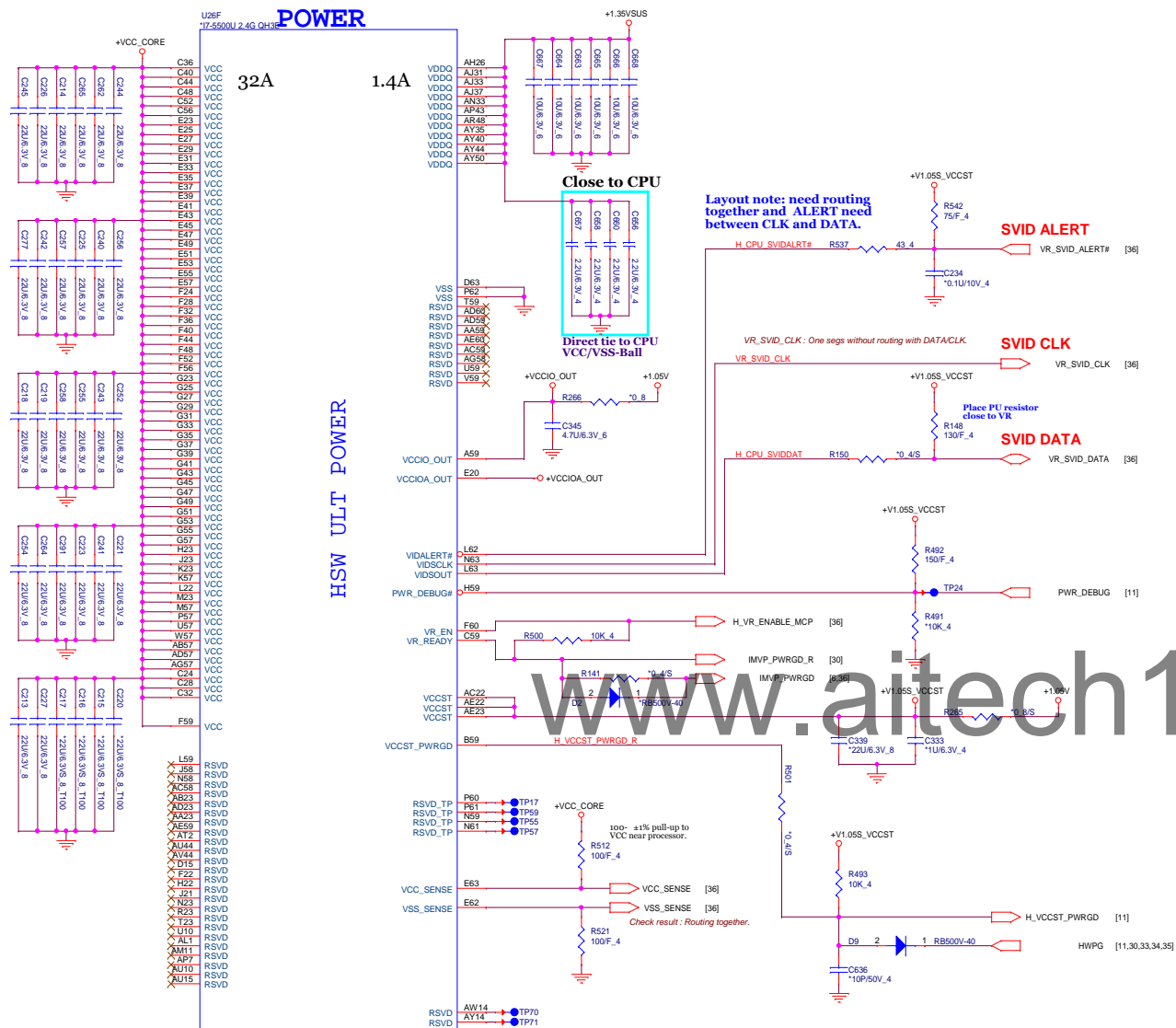
The PECI interface is a controlled and reliable one-wire bi-directional signal which is used to communicate the temperature of the Broadwell processor digital thermometer to the PECI host controller or to monitor and control the Broadwell processor information such as energy, power limits, status and DDR temperature.



Haswell ULT Processor (DDR3L)

[12] M_A_DQ[63:0]
[13] M_B_DQ[63:0]
[12] M_A_DQS[7:0]
[12] M_A_DQSP[7:0]
[13] M_B_DQS[7:0]
[13] M_B_DQSP[7:0]





Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

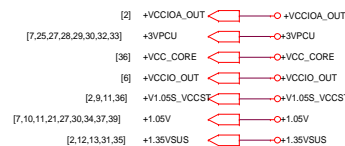
	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

* The CFG signals have a default value of "1" if not terminated on the board.

* CFG[3] : MSR Privacy Bit Feature,

"0" = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden.)

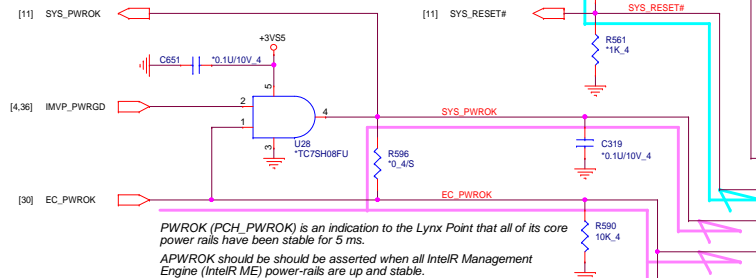
```
* CFG[4]: eDP enable. ( " 1 " = Disabled, " 0 " = Enabled )
```



Lynx Point-LP Platform Controller Hub (LVDS,DDI)

System PWR_OK(CLG)

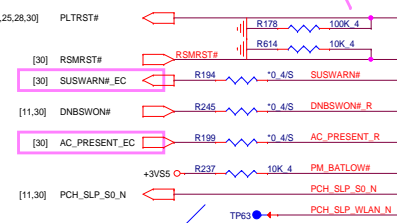
SYS_PWROK is used to inform the Lynx Point that power is stable to some other system component(s) and the system is ready to start the exit from reset.



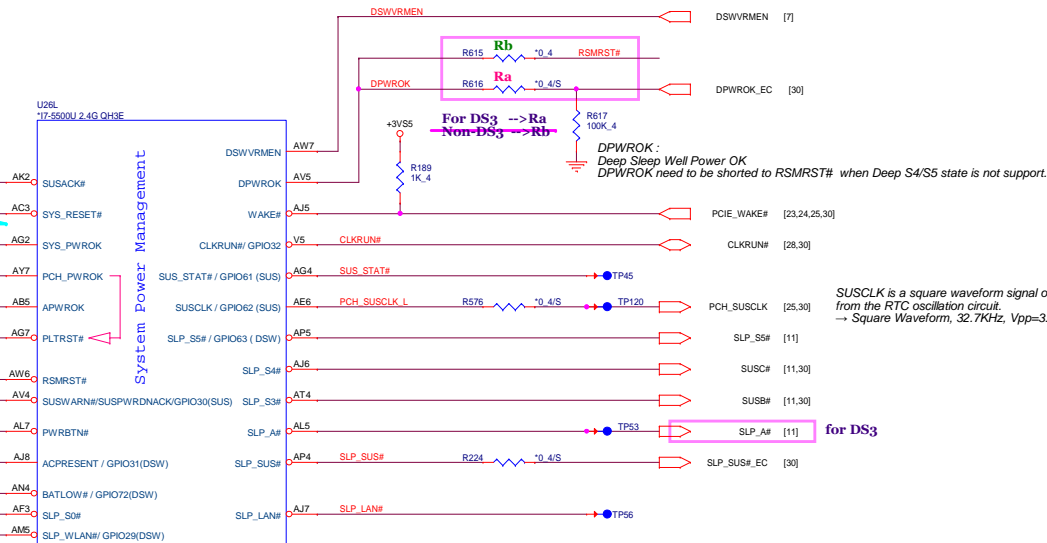
APWROK (PCH_PWROK) is an indication to the Lynx Point that all of its power rails have been stable for 5 ms.

APWROK should be asserted when all Intel® Management Engine (Intel® ME) power-rails are up and stable.

SUSPWRDNACK / SUSWARN#
This signal is Active-high and is driven low by the Intel® ME for DS3 when it requires the PCH Suspend Well to be powered.



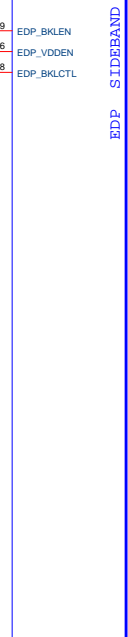
SLP_S0# is a PCH signal which indicates the system is in the S0ix State. SLP_S0# stays high in Sx and during Sx entry/exit. This signal will be low during low power state.



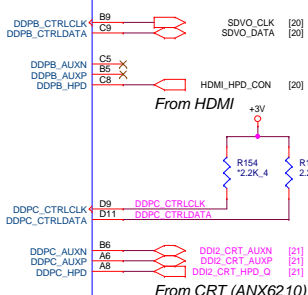
SUSCLK is a square waveform signal output from the RTC oscillation circuit.
→ Square Waveform, 32.7KHz, Vpp=3.3V.

for DS₃

LP_S0# is a PCH signal which indicates the system is in the S0ix State.
LP_S0# stays high in Sx and during Sx entry/exit. This signal will be low during low power state.



EDP SIDEBAND

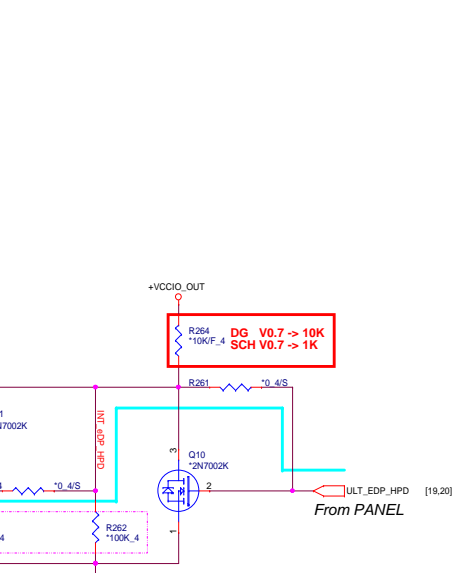


From HDMI +3V

From CRT (ANX6210)

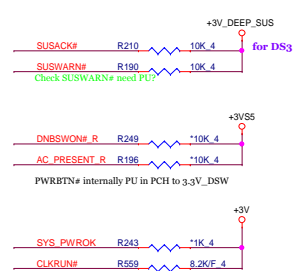
INT. HDMI

DP TO VGA



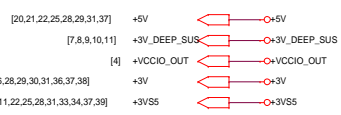
EDP_HPD need pull down via 100KΩ, so combine with
RTD2136 pin-1 DP_HPD pull down resistor.
If only for eDP panel, EDP_HPD must stuff one 100KΩ.

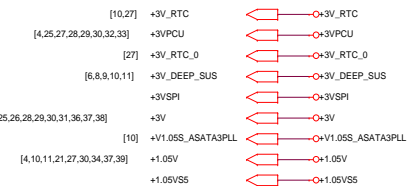
PCH Pull-high/low(CLG)



PWRBTN# internally PU in PCH to 3.3V_DSW

SYS_PWROK R243 *1K_4
 CLKRUN# R559 8.2K/F_4





Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

Cardreader

WLAN

LAN

GPU

Card Reader

WLAN

LAN


VGA

CLK_REQ/Strap Pin(CLG)

PCI/USB0# Pull-up(CLG)

for DS3

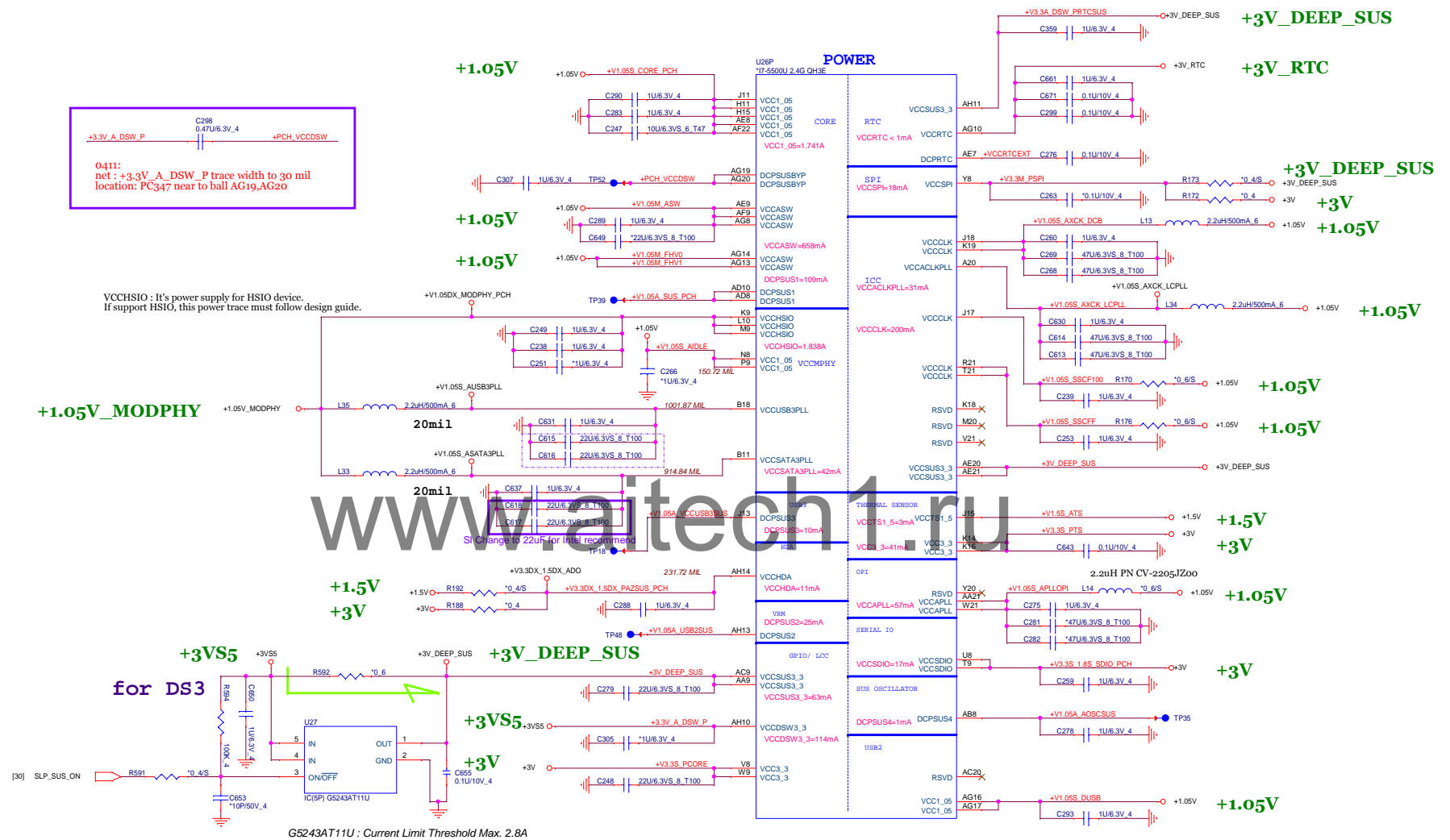
20141027A-DGPU_HOLD_RST# will make VGA_RST# has a pulse during boot when PU +3V. So change to PD.















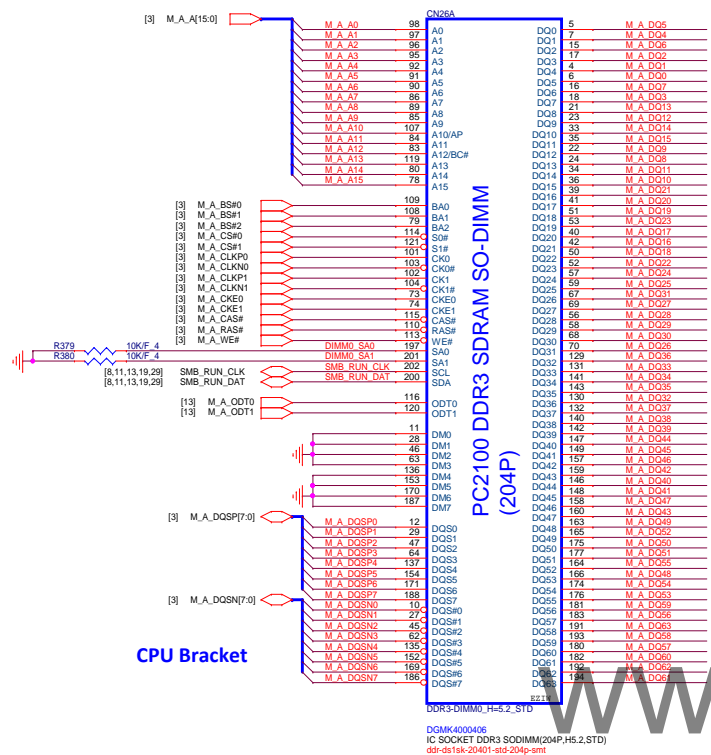
Quanta Computer Inc.
PROJECT : TWB & JWV (MB)

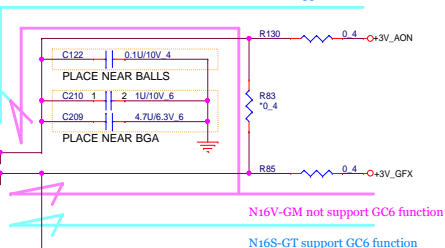
Size	C	Document Number	ULT 7/9 (PCIE/USB/CLK)	Rev.	2A
Date:	Monday, November 24, 2014			Sheet :	8 of 44



```
Lynx Point-LP Platform Controller Hub
(HDA,JTAG,SATA)(POWER)
```

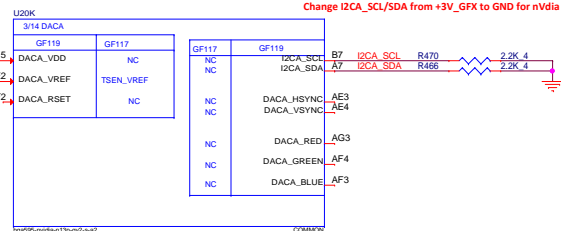


- | | | | |
|---------------------------------|----------------------|---|----------------------|
| [37] | +V1.05D_X_MODPHY_PCH |  | +V1.05D_X_MODPHY_PCH |
| [37] | +1.05V_MODPHY |  | +1.05V_MODPHY |
| [8] | +V1.05S_AXCK_LCPLL |  | +V1.05S_AXCK_LCPLL |
| | +V3.30X_1.50X_ADO |  | +V3.30X_1.50X_ADO |
| [8] | +V1.05S_AUSB3PLL |  | +V1.05S_AUSB3PLL |
| [7] | +V1.05S_ASATA3PLL |  | +V1.05S_ASATA3PLL |
| [6,7,8,9,11] | +3V_DEEP_SUS |  | +3V_DEEP_SUS |
| | [22,25,26,34] |  | +1.5V |
| 25,26,28,29,30,31,36,37,38] | +3V |  | +3V |
| 6,9,11,22,25,28,31,33,34,37,39] | +3V5S |  | +3V5S |
| | [7,27] |  | +3V_RTC |
| [4,7,11,21,27,30,34,37,39] | +1.05V |  | +1.05V |

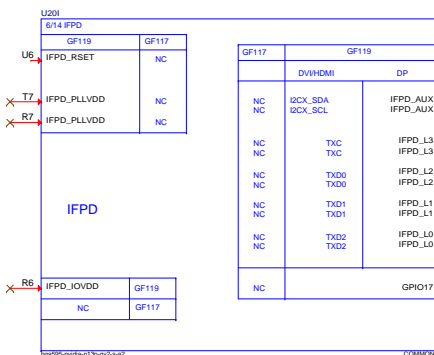




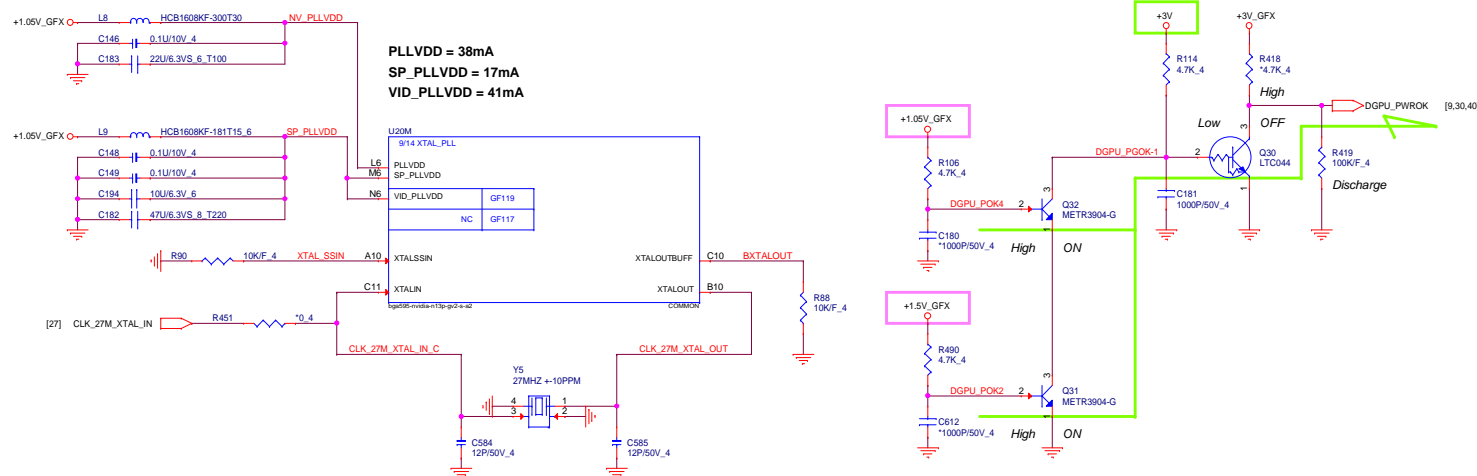
 Quanta Computer Inc. PROJECT : TWB & JWV (MB)		
Size	Document Number	Rev.
C	N16x-PCIe & Power-1	2A
Date:	Monday, November 24, 2014	Sheet : 14 of 44



GPI/O	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



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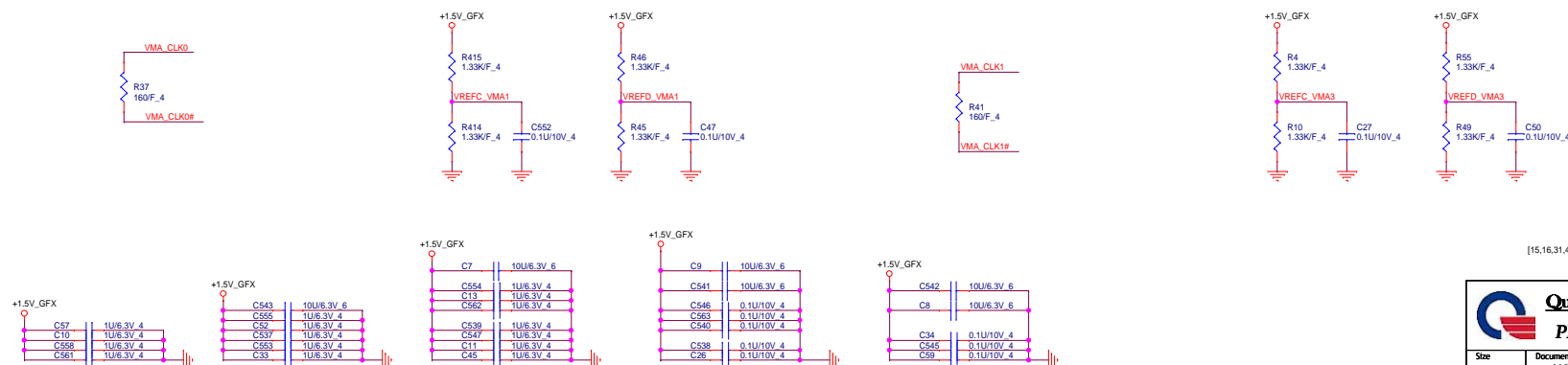
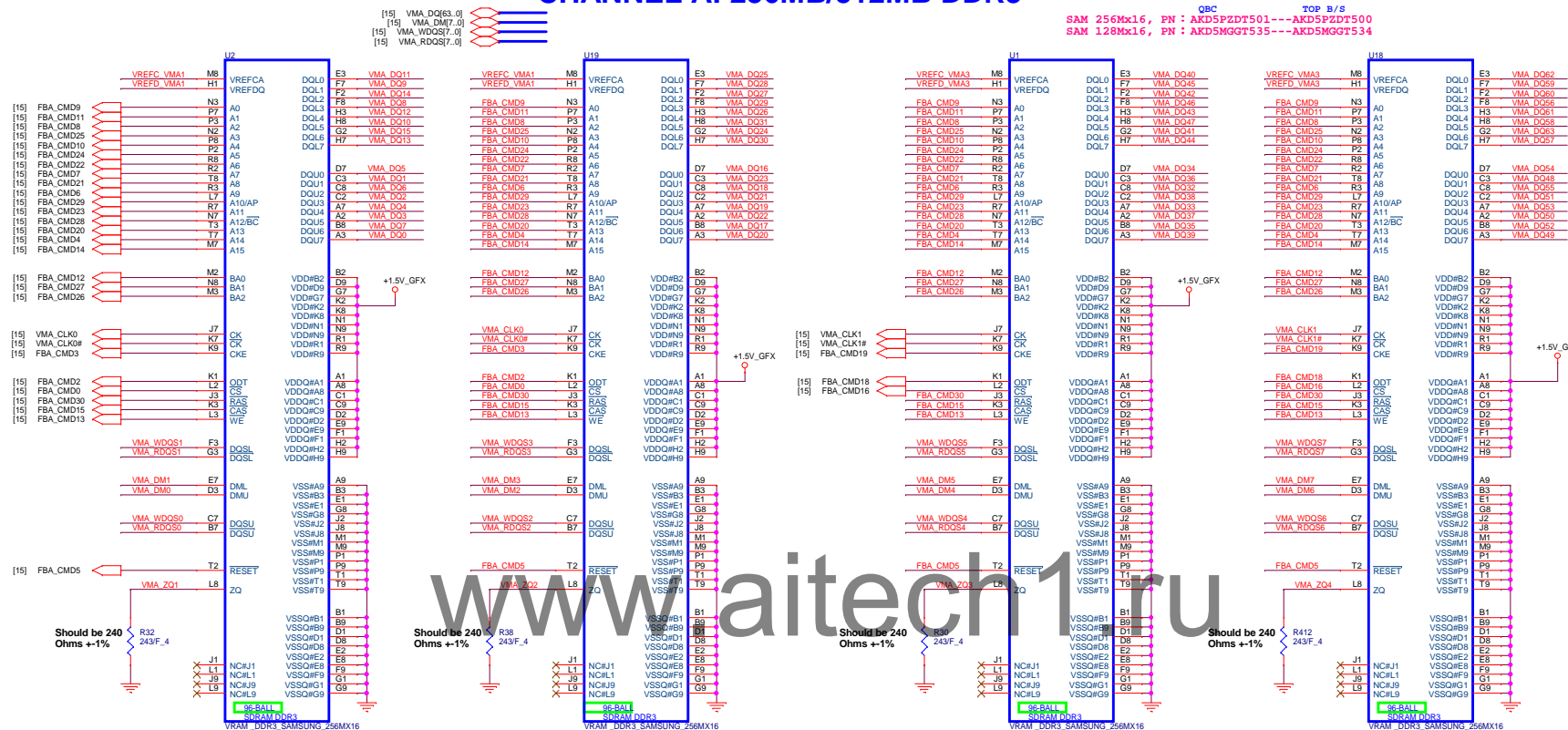


CHANNEL A: 256MB/512MB DDR3

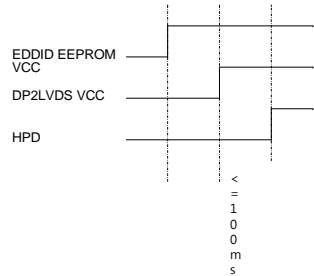
```

HYU 256Mx16, PN : AKD5PGWTW08---AKD5PGWTW07
HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02
                QBC                TOP B/S
SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500
SAM 128Mx16, PN : AKD5MGGT535---AKD5MGGT534

```



RTD2136S Power Up Sequence



AUX Channel : 6inch/85Ω

Main Link : 6inch/85Ω

[8,30] MBCLK2

[8,30] MBDATA2

[8,11,12,13,29]

[8,11,12,13,29]

5.1 Power On/Off Sequence

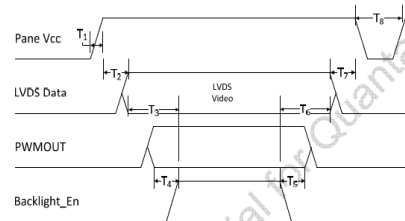


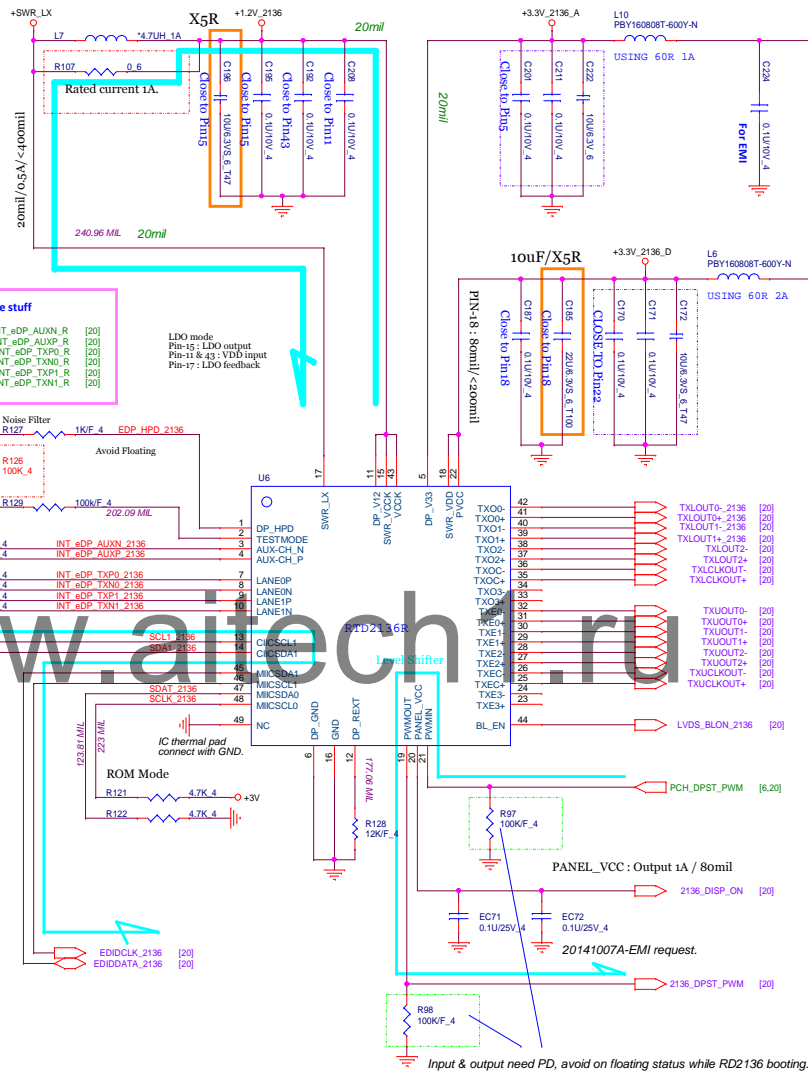
Figure 5-1 Panel On/Off Sequence

Table 5-1 Timing parameters of Power On/Off Sequence

Time Para.	Description	Min.(ms)	Max.(ms)
T ₁	Rising time of Panel Vcc	0.5	10
T ₂	Delay from Panel Vcc output enable to LVDS output enable	0	50
T ₃	Delay from LVDS output enable to backlight output enable	200	—
T ₄	Delay from PWM output enable to backlight output enable	0	—
T ₅	Delay from backlight output enable to PWM output enable	0	—
T ₆	Delay from backlight output enable to LVDS output enable	200	—
T ₇	Delay from LVDS output enable to Panel Vcc output enable	0	50
T ₈	Delay between two power on/off sequence	500	—

SWR MODE	LDO MODE
Stuff Inductance	Stuff Resistor

L7: need use CV-4709MN00 for Vendor suggestion



LVDS (RTD2136-CNN) : 7inch/90-100Ω

PIN-20 PANEL_VCC

The switch can support any panel resolution with the maximum current consumption below 1-A, and can endure panel inrush current up to 2-A.

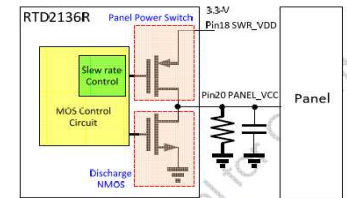


Figure 4 The application of Panel Power Switch

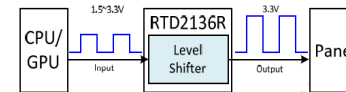
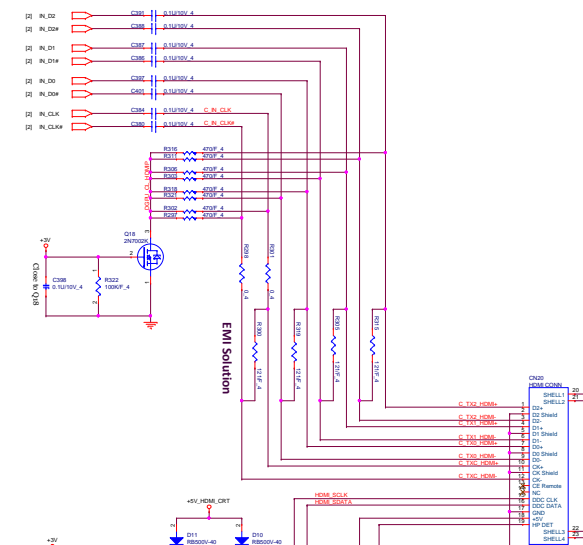


Table 5 Level Shifter Specification

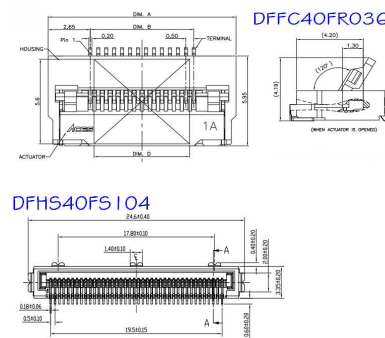
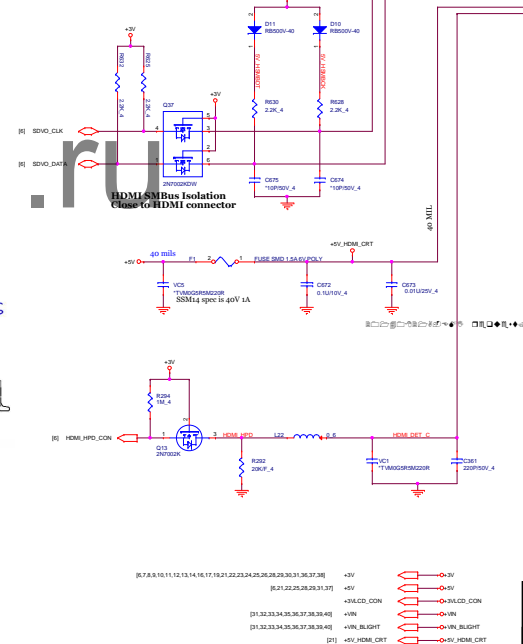
Parameter	Symbol	Min	TYP	MAX	UNITS
Input High Voltage	V _{IH}	1.25	1.5	3.6	V
Input Low Voltage	V _{IL}	—	—	0.8	V
Operation Frequency	F _{max}	—	—	3	MHz

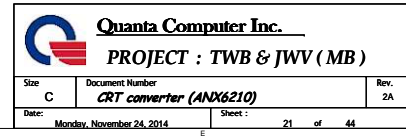
[6,7,8,9,10,11,12,13,14,16,17,19,20,21,22,23,24,25,26,28,29,30,31,36,37,38]

+3V

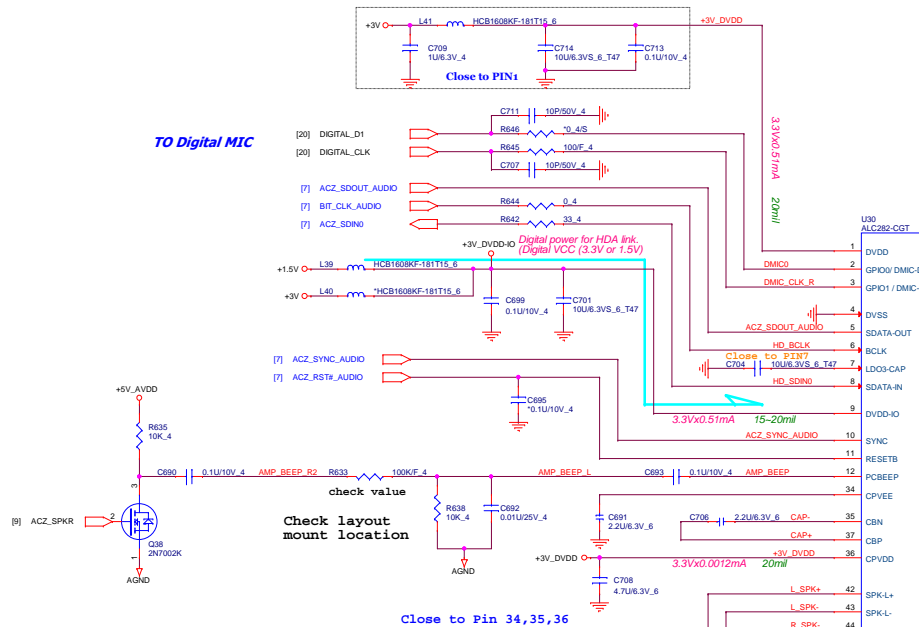


HDMI Conn.
HDMI follow JWU

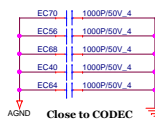
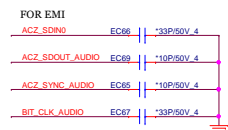




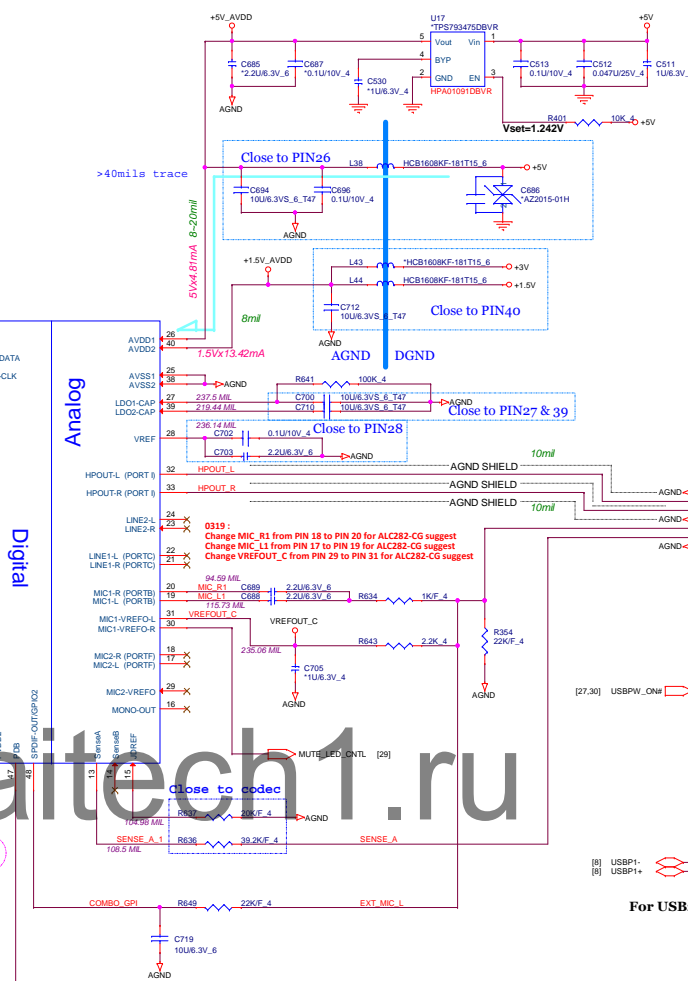
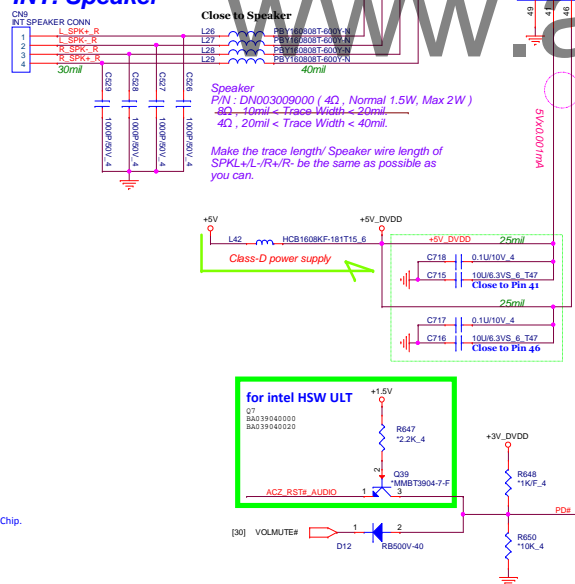
TO Digital MIC



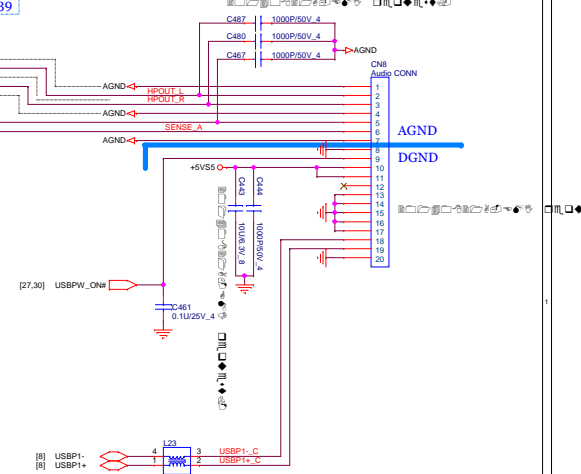
INT. Speaker



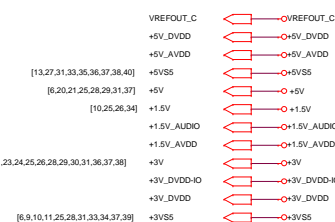
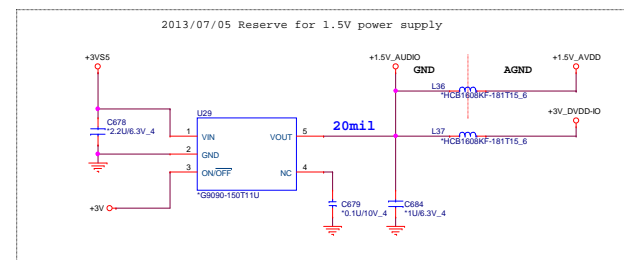
place to near Audio Chip or under Audio Chip.



USB 2.0 & AUDIO COMBO JACK



For USB2.0 Port on Right Side



9. Power Sequence

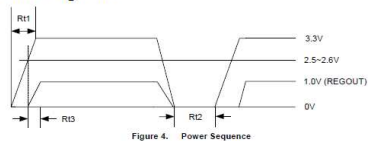


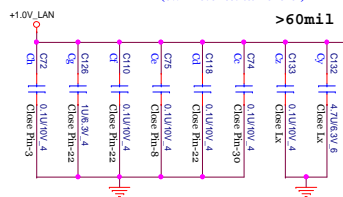
Table 16. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Ra1	3.3V Rise Time	0.5	-	100	ms
Ra2	3.3V Off Time	50	-	-	ms
Ra3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3,8,22,30
Place Cg & Ch close to each VDD10 pin22

RTL8111GS stuff Lx,Cy,Cz
(SWR mode need stuff Cx & Cz)



RTL8111GS stuff Cc, Cd
Remove For Not Using SWR mode
Stuff Cc and Cd only, close to each VDD33 pin-- 11, 32
Place Cc and Cd close to each VDD33 pin-- 23

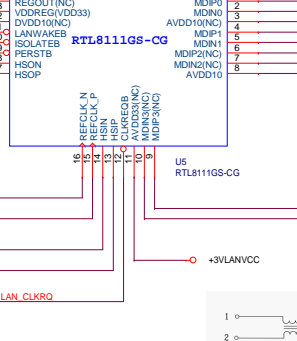
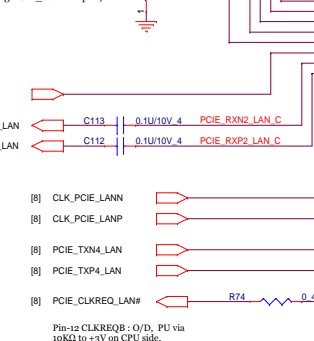
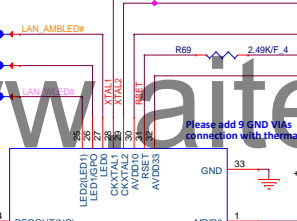
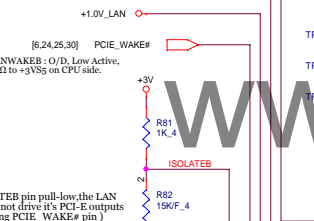
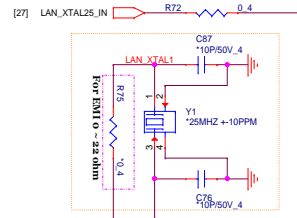
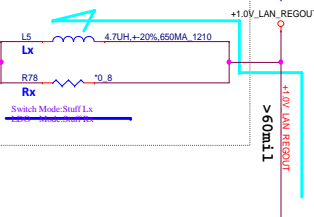
[6,11,14,21,24,25,28,30] PLTRST#

Differential Impedance : 100Ω

Differential Impedance : 100Ω

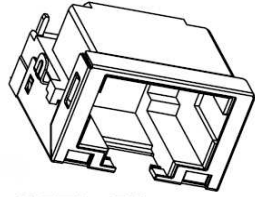
Power trace Layout 宽度> 60mil
Trace<30 mil
Width > 60 mil

RTL8111GS Pin-24 REGOUT : Switching Regulator 1.0V Output.

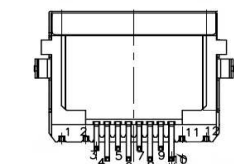
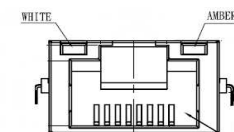


Pin	Name	Description	Cable Color
1	TX_D1+	Tranceive Data+	white/green
2	TX_D1-	Tranceive Data-	green
3	RX_D2+	Receive Data+	white/orange
4	BI_D3+	Bi-directional Data+	blue
5	BI_D3-	Bi-directional Data-	white/blue
6	RX_D2-	Receive Data-	orange
7	BI_D4+	Bi-directional Data+	white/brown
8	BI_D4-	Bi-directional Data-	brown

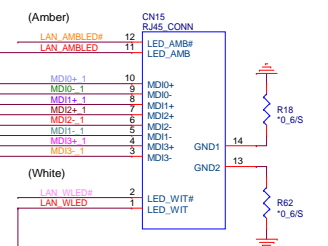
TX_D1+
TX_D1-
TX_D2+
TX_D3+
TX_D3-
TX_D2-
TX_D4+
TX_D4-



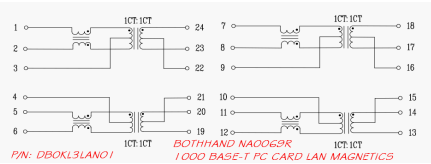
DFTJ12FR330



LAN conn

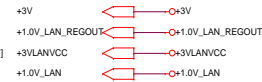


20140930A-Transformer must H<2.5mm,
so change source & pin define.



DBOKL3LAN01 TRANSFORMER KL3 LAN(NA0069R LF)
DBOKL3LAN02 TRANSFORMER KL3 LAN(NS692417)

[6,7,8,9,10,11,12,13,14,16,17,19,20,21,22,24,25,26,28,29,30,31,36,37,38]

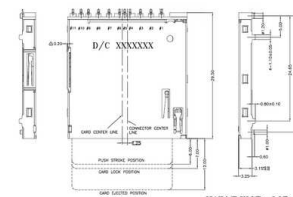


RTL8111GS : Switching Regulator
RTL8111G : LDO Regulator

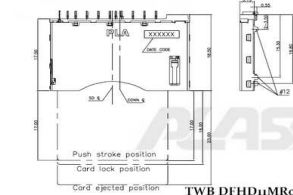
Quanta Computer Inc.
PROJECT : TWB & JWV (MB)

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Date:	Monday, November 24, 2014			Sheet :	23 of 44

Follow JW5



CARD READER For TWB 15"



DFHS11FR153 : TWB (15")
DFHD11MR052 : JWV (14")

PIN-15	SP1	SD_D1	---	I/O	SD Data 1 (SD_D1)
PIN-16	SP2	SD_Do	MS_D1	I/O	SD Data 0 (SD_Do)
PIN-17	SP3	SD_CLK	MS_Do	1/0	SD Clock signal (SD_CLK)
PIN-19	SP4	SD_CMD	MS_D2	1/0	SD CMD signal (SD_CMD)
PIN-20	SP5	SD_D3	MS_D3	1/0	SD Data 3 (SD_D3)
PIN-21	SP6	SD_D2	MS_CLK	1/0	SD Data 2 (SD_D2)
PIN-29	SP7	SD_WP	MS_BS	I	SD Write Protect signal
PIN-30	SD_CD#	SD_CD#	---	I	SD Card Detection signal



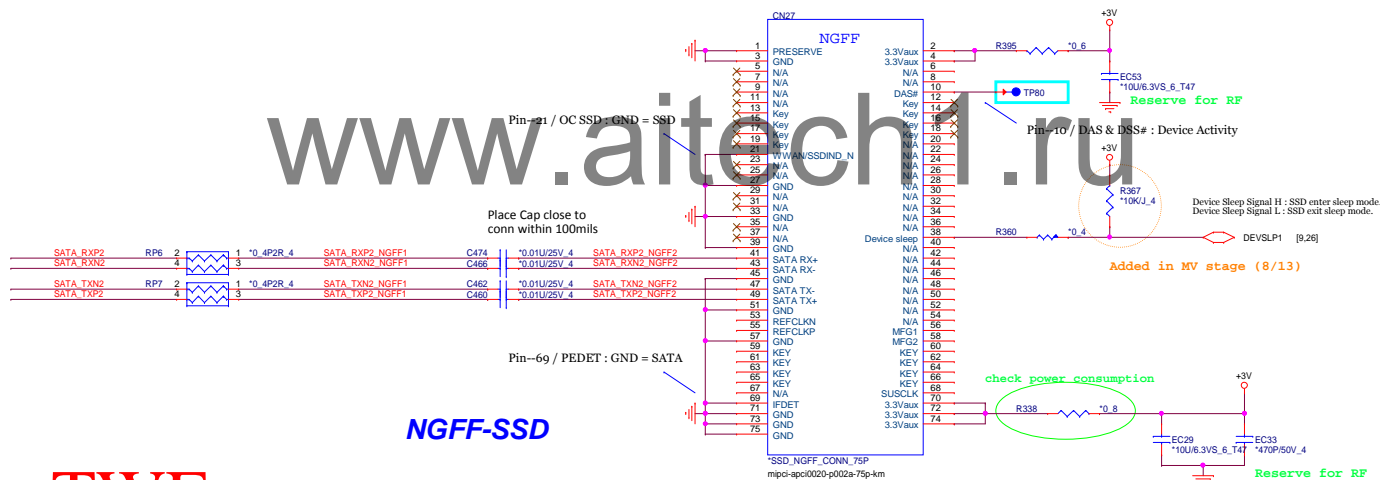
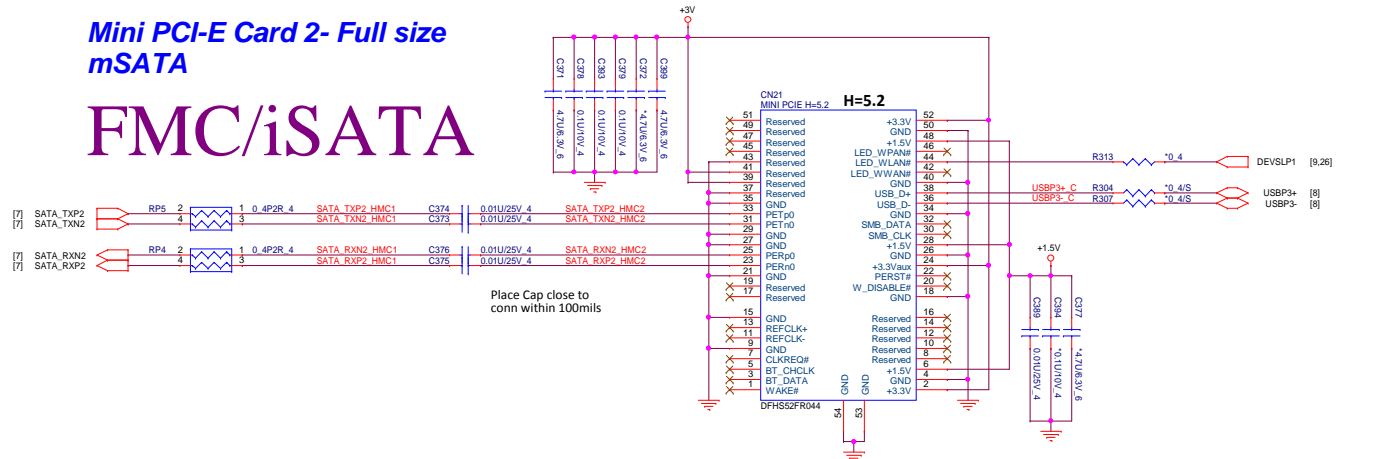
(Reserve)



Size C	Document Number HMC WLAN & NGFF WLAN	Rev. 2A
Date: Monday, November 24, 2014	Sheet : 25 of 44	

Mini PCI-E Card 2- Full size mSATA

FMC/iSATA



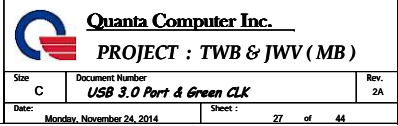
Follow TWE
2280/2242

20140808-Change P/N & FP, must confirm pin define again.

mipci-apci0018-p002a-75p-kb

Input Voltage	Parameter	32GB	64GB	128GB	256GB	512GB
5V ± 5%	SATA 6Gb/s host interface					
	Read [mW]	NA	2,600	2,700	2,900	TBD
	Write [mW]	NA	2,200	2,350	4,800	TBD
3.3V ± 5%	Read [mW]	2,200	2,450	2,650	2,650	NA
	Write [mW]	2,100	2,150	3,400	4,500	NA

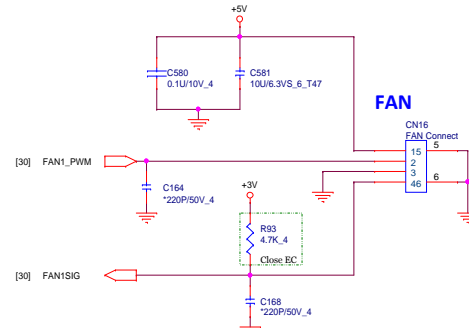
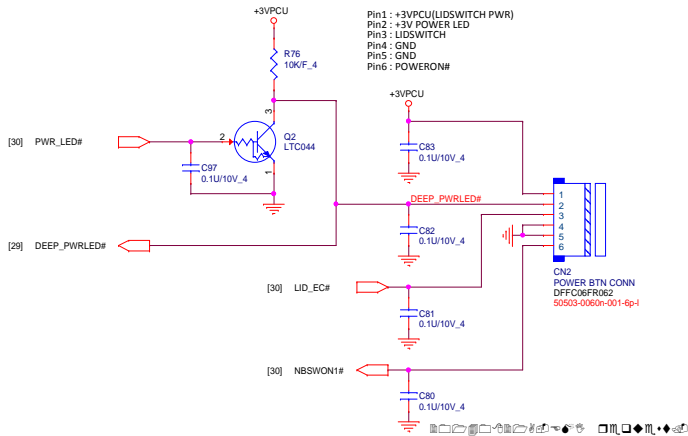
Table 3-3: SanDisk SSD X110 Average Max Power Consumption



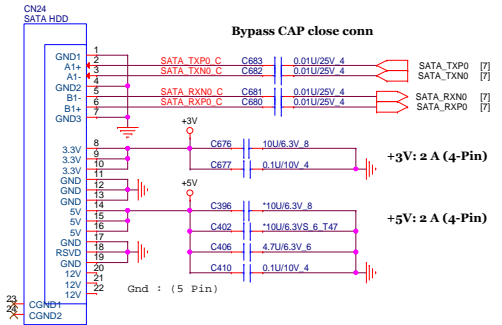
0927:
DEL Touch Pad Connector CN7 for U83 Change CN4 PIN2 from +3V to DEEP_PWRLED# for Power LED

Power Button Connector

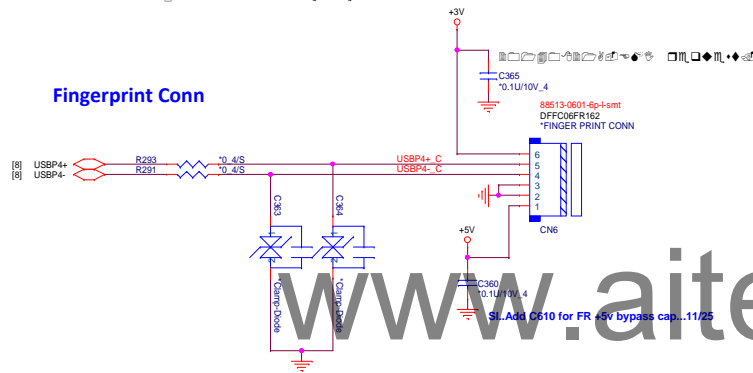
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



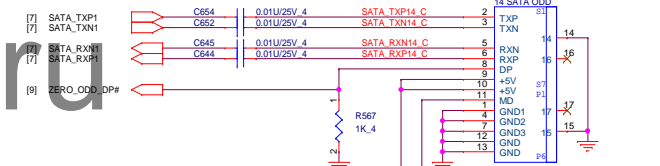
SATA HDD Connector



Fingerprint Conn

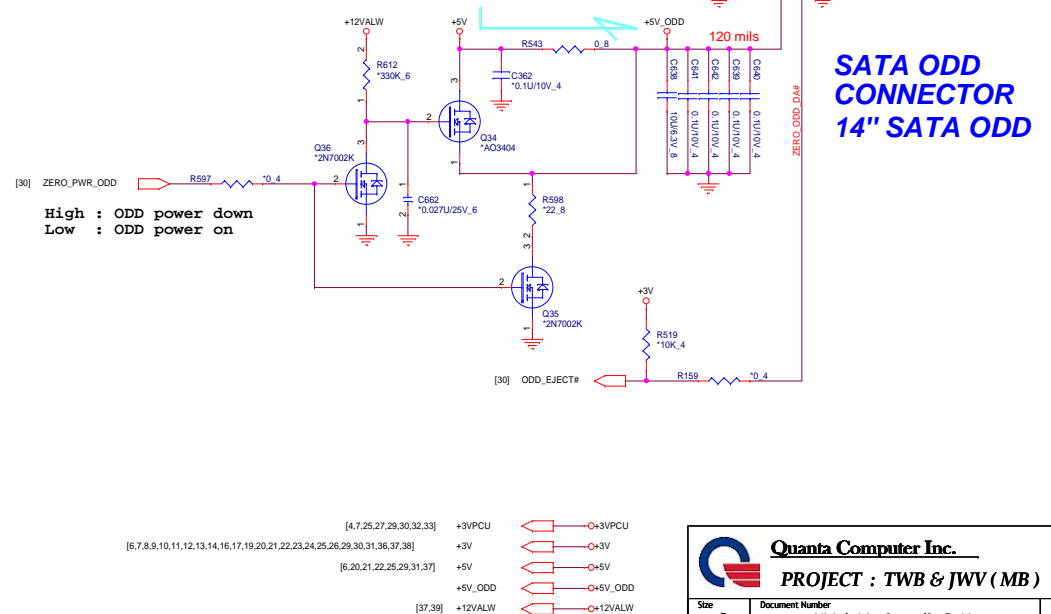
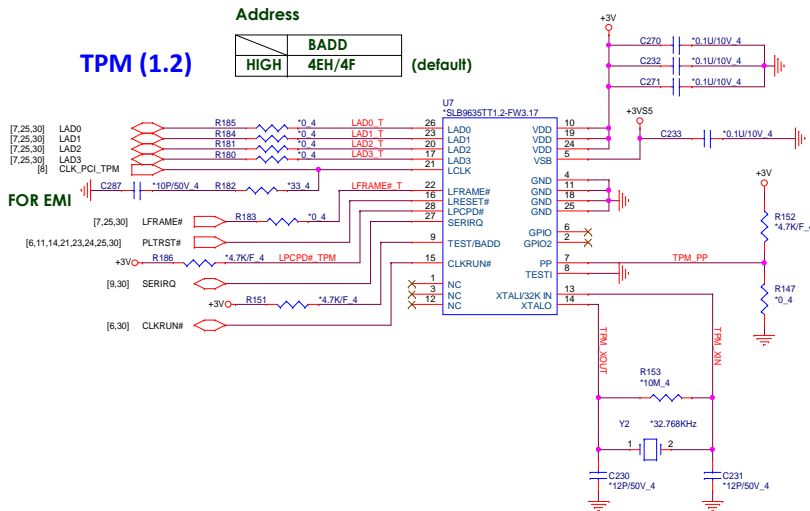


Bypass CAP close conn



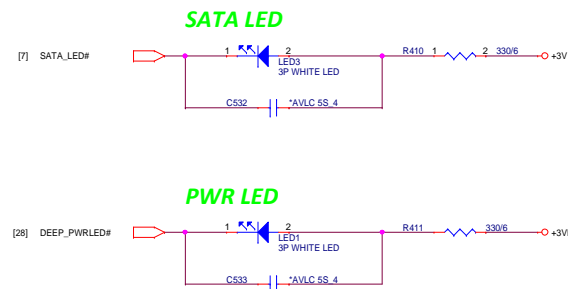
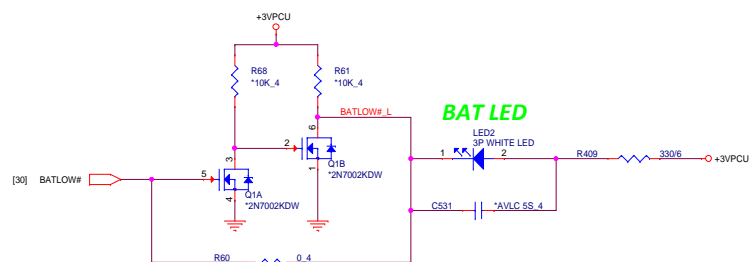
TPM (1.2)

Address	BADD
HIGH	4EH/4F (default)

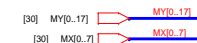


JWV remove G-sensor/Touch Screen function.

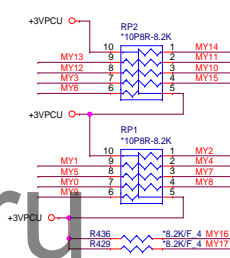
2013/07/05 Reserve for BATTERY LED



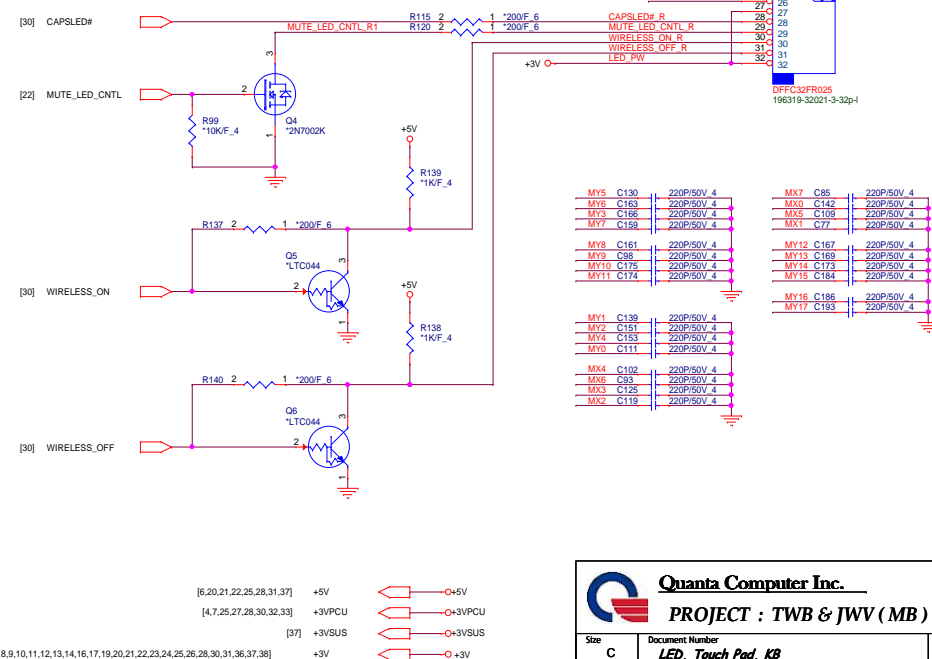
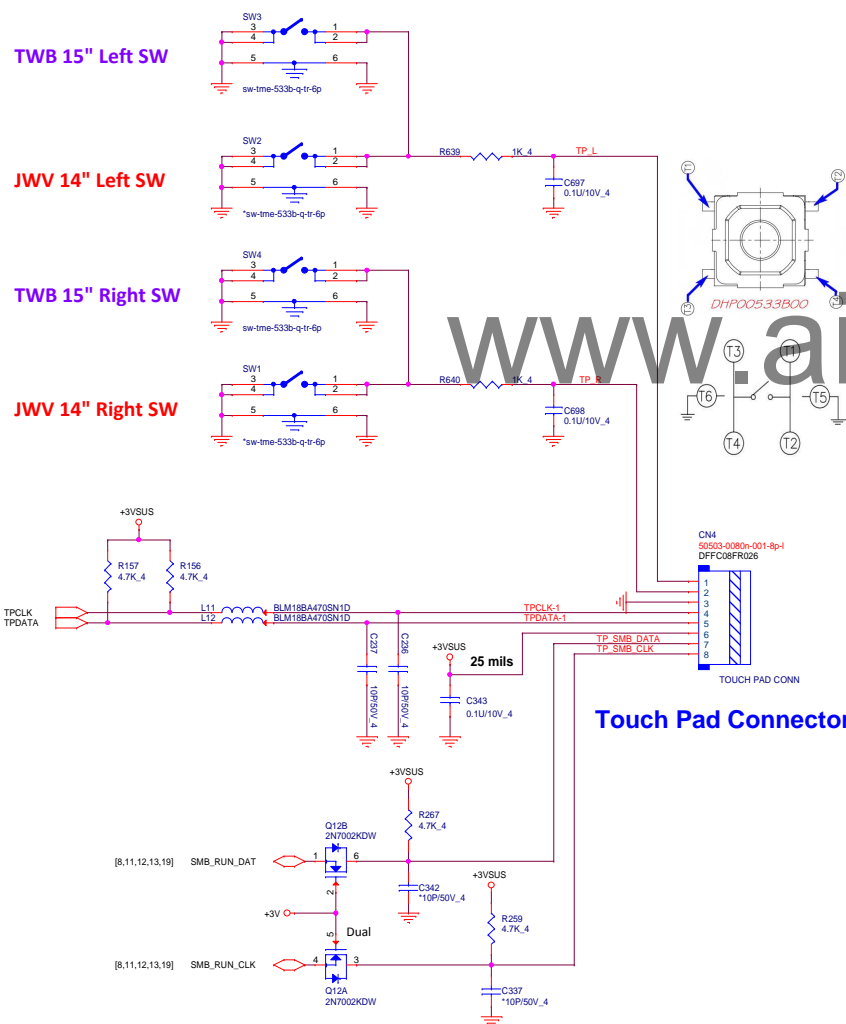
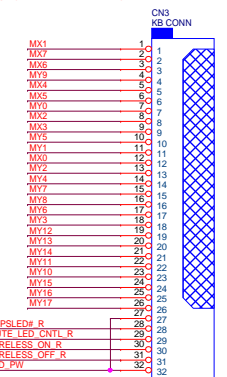
KEYBOARD Con.

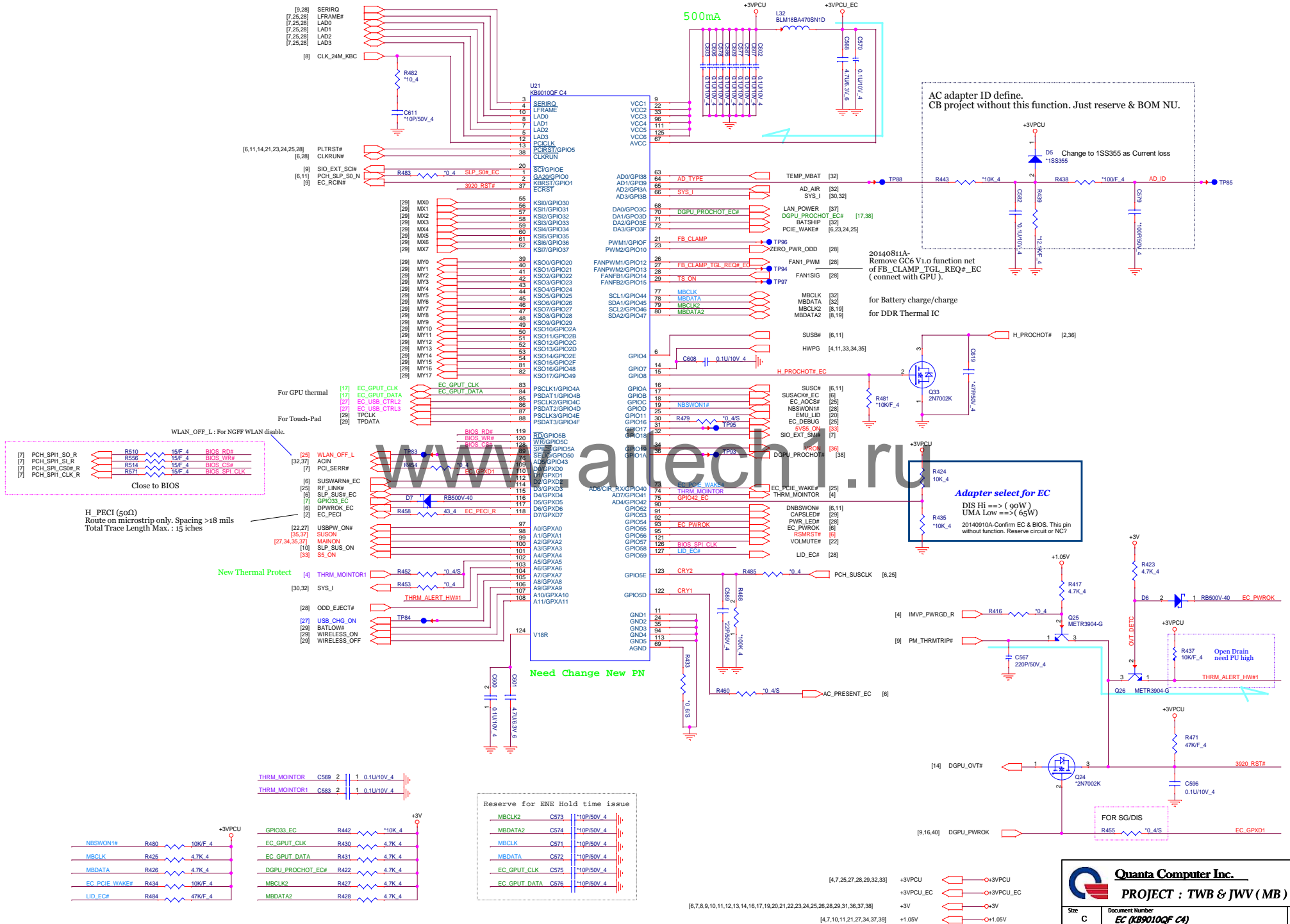


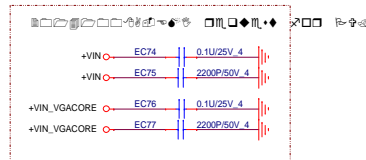
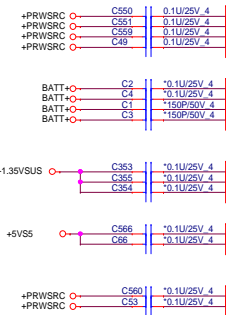
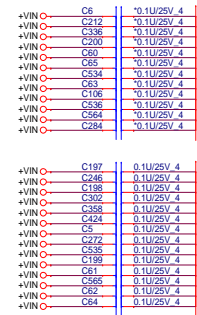
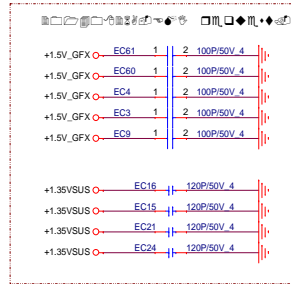
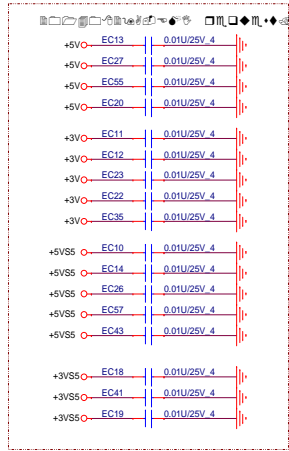
KEYBOARD PULL-UP



0503 :
Change pin define and M/B keyboard connector follow R33



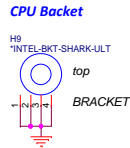




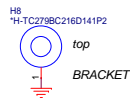
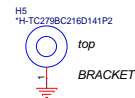
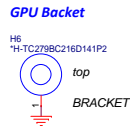
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Hole

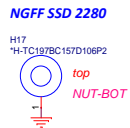
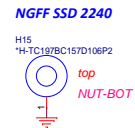
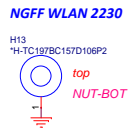
CPU BRACKET
P/N : FBUS6017010



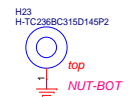
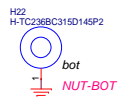
GPU BRACKET
P/N : FBR62021010



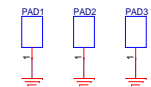
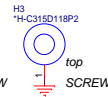
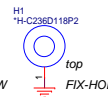
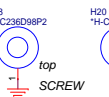
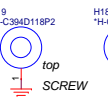
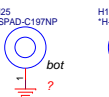
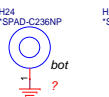
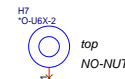
NGFF NUT
P/N : MBY01001010

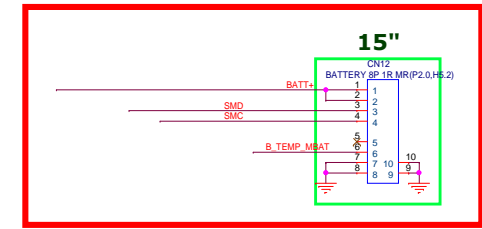


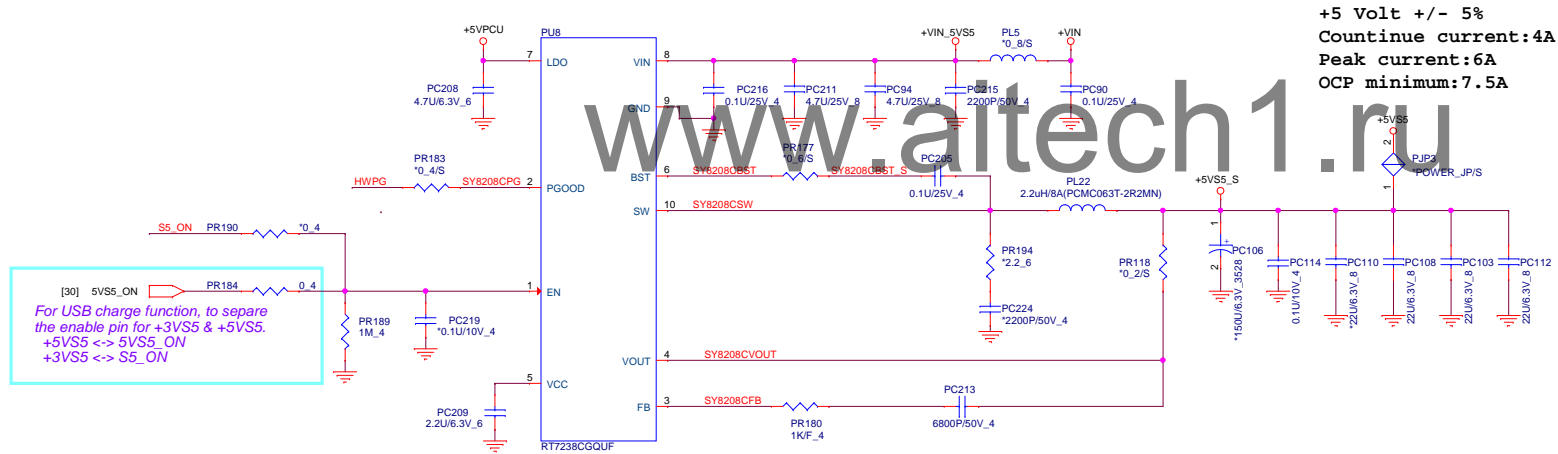
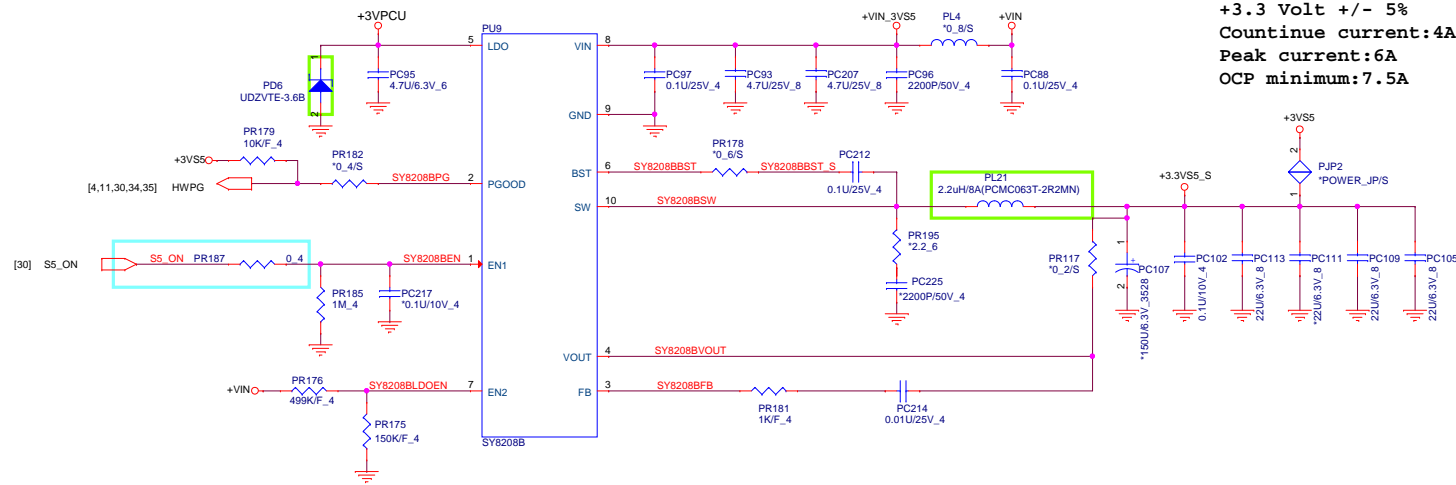
FAN NUT
P/N : MBFF4001010

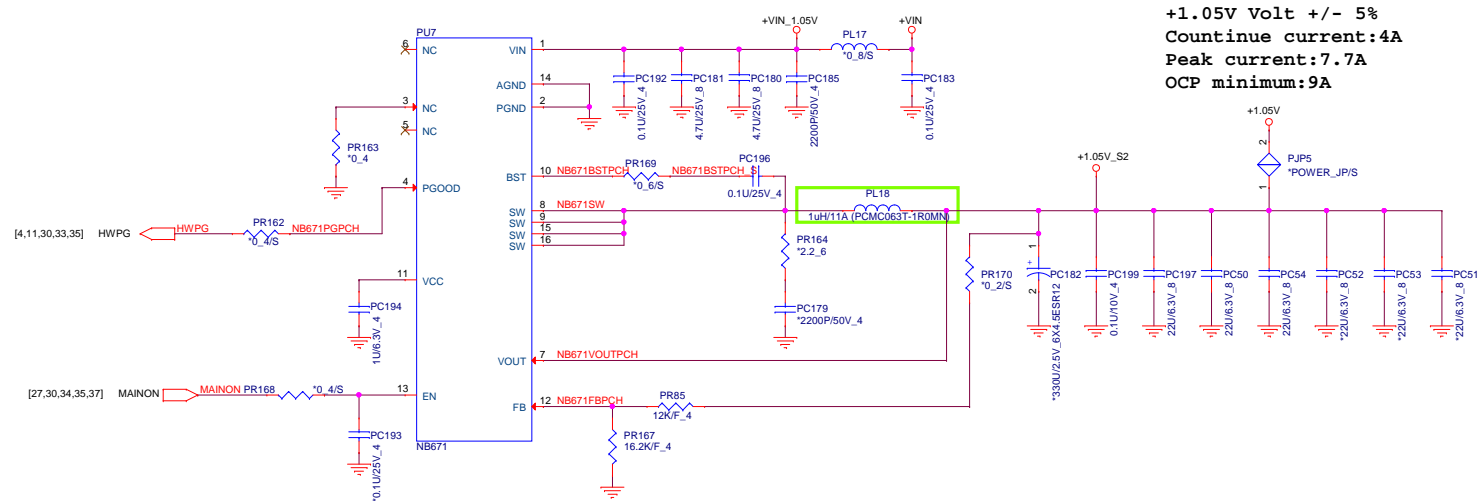


Thermal Module



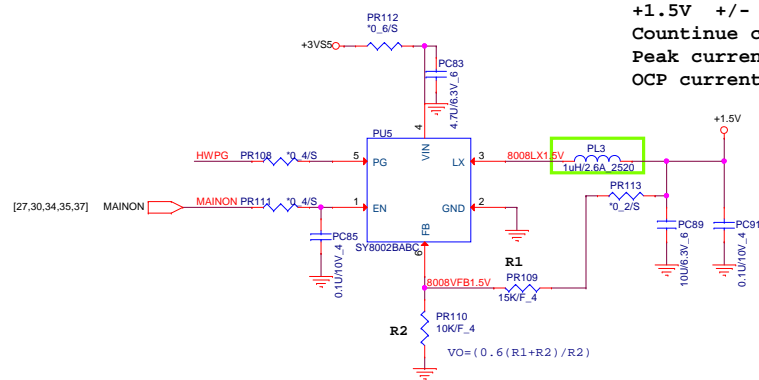








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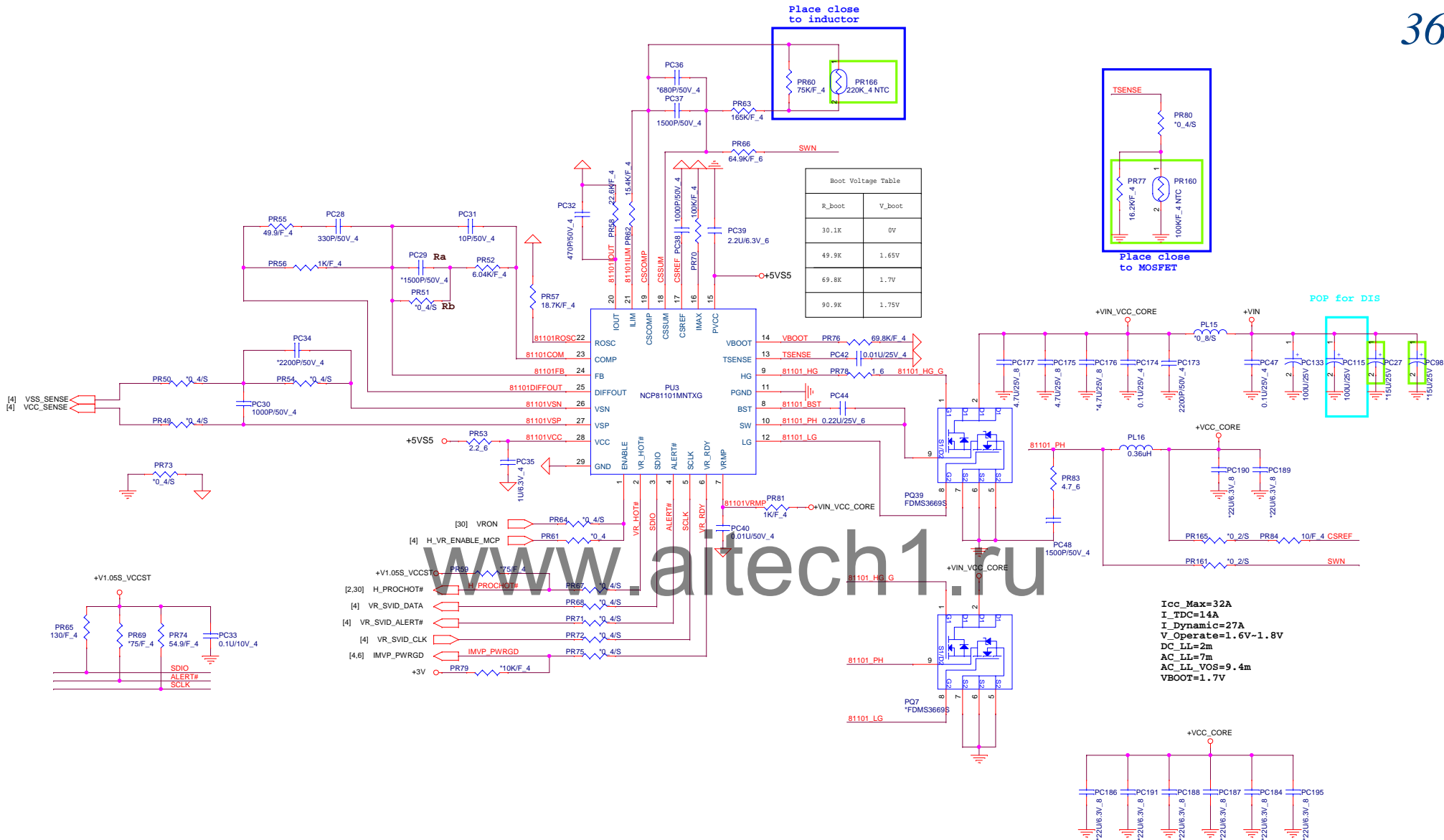
+1.5V +/- 5%
Continue current:1.3A
Peak current:1.5A
OCP current:2A

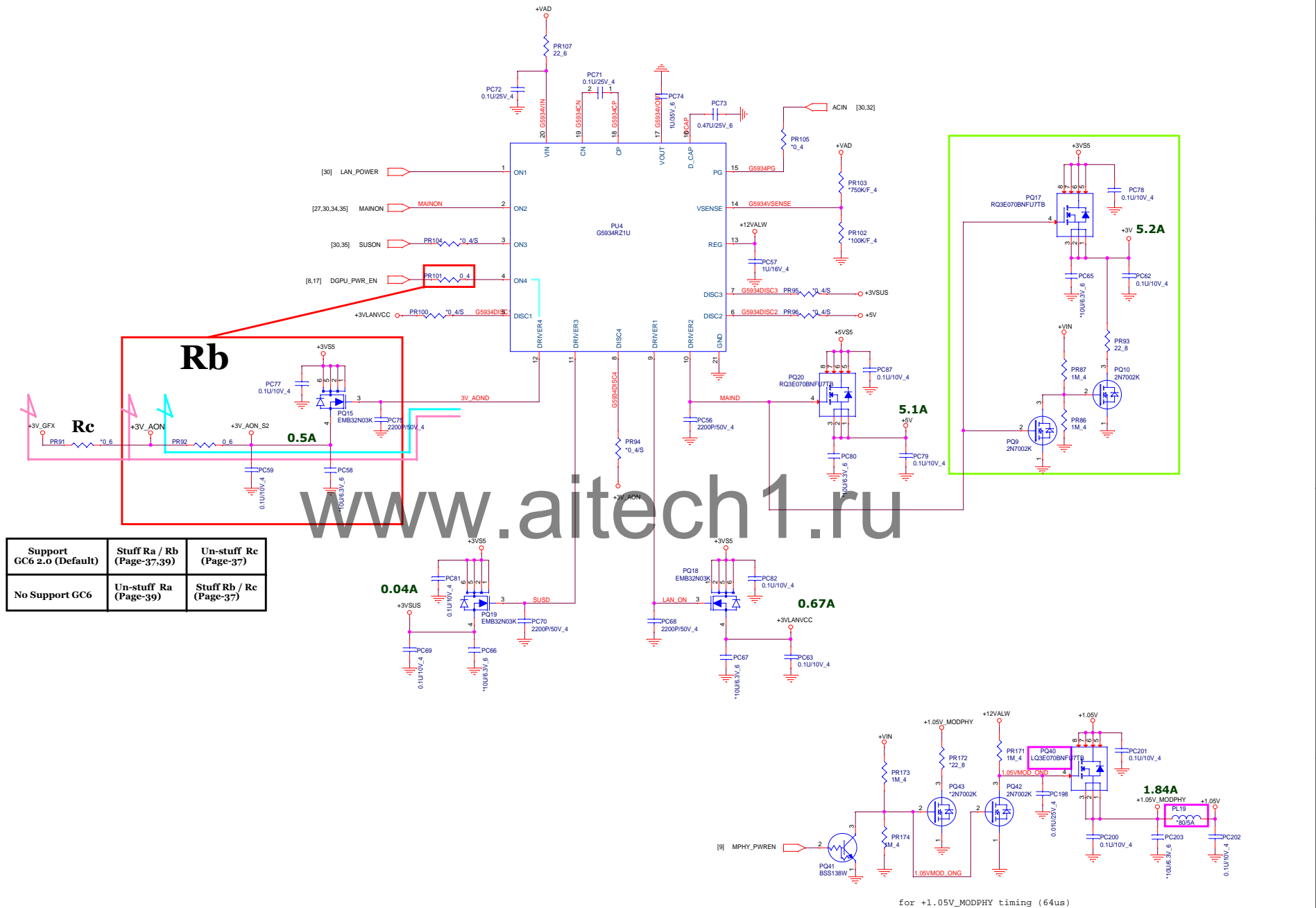


	+VIN	[20,31,32,33,35,36,37,38,39,40]
	+3VS5	[6,9,10,11,22,25,28,31,33,37,39]
	+5VS5	[13,22,27,31,33,35,36,37,38,40]
	+5VPCU	[13,33]



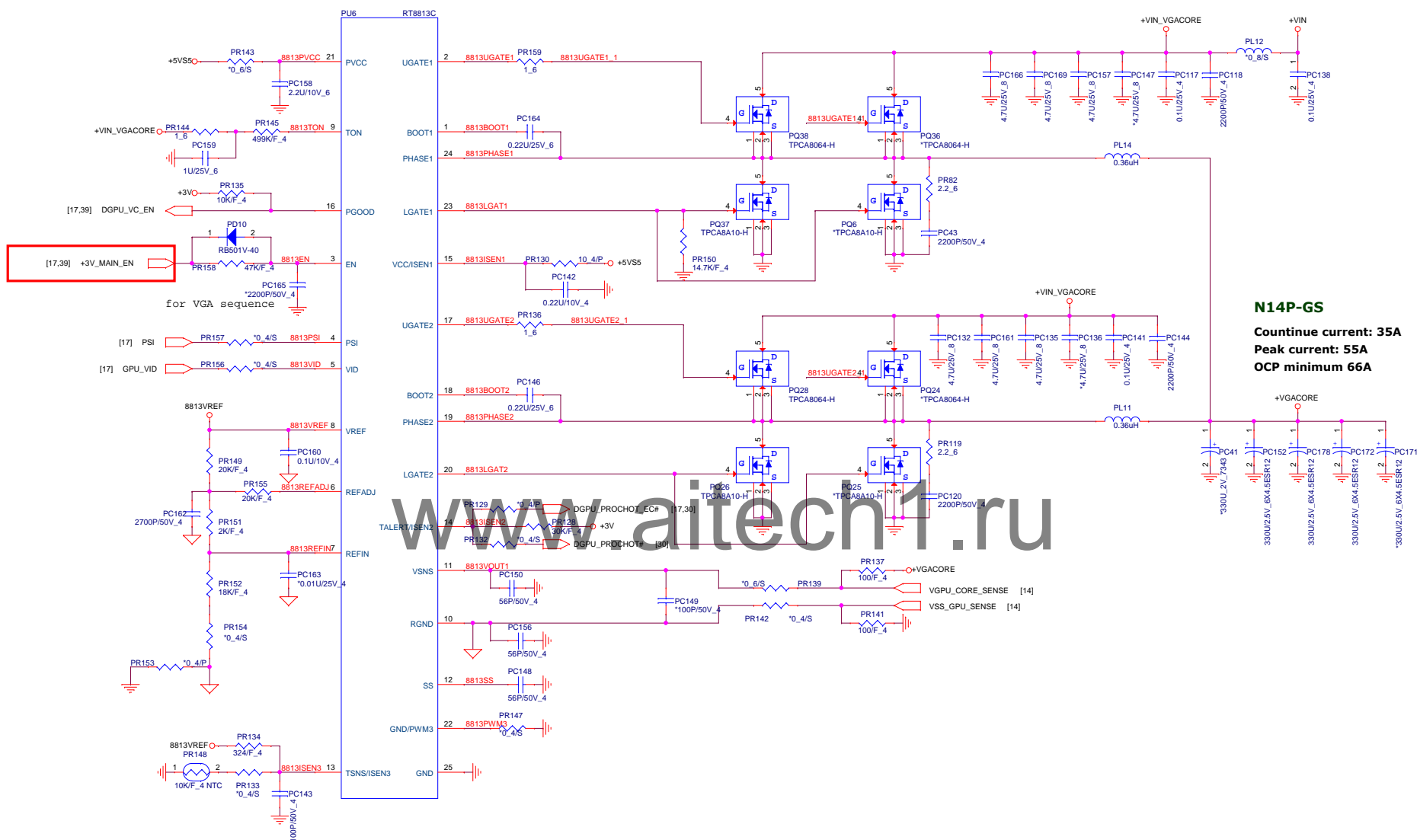
	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



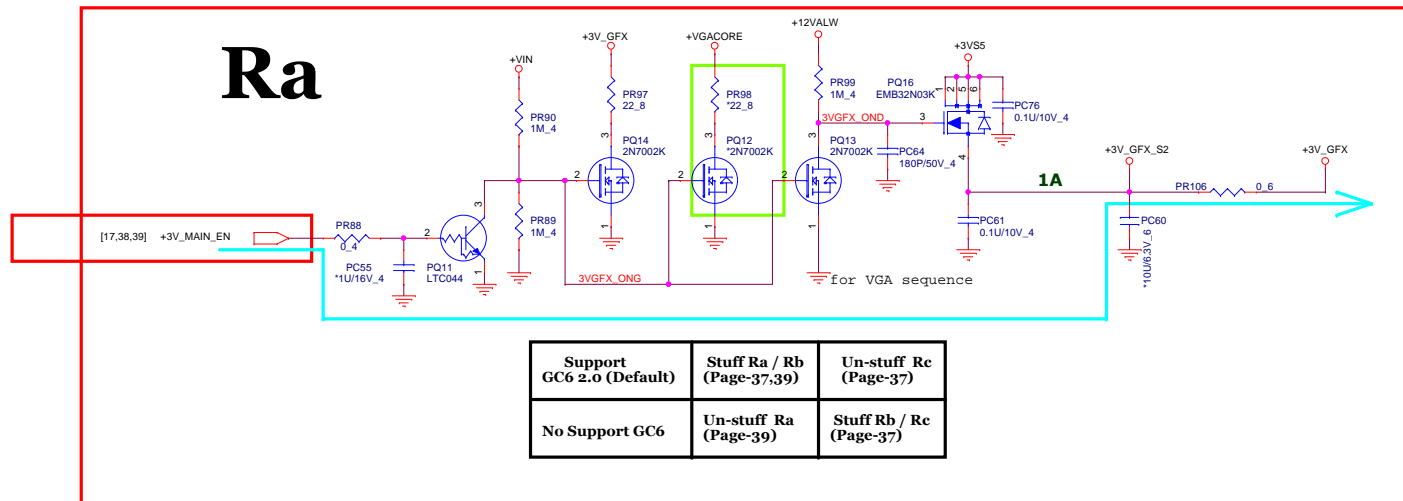


[6,7,8,9,10,11,12,13,14,16,17,19,20,21,22,23,24,25,26,28,29,30,31,36,38]
 [6,20,21,22,25,28,29,31]
 [20,31,32,33,34,35,36,38,39,40]
 [6,9,10,11,22,25,28,31,33,34,39]
 [13,22,27,31,33,35,36,38,40]
 [28,36]
 [23,27]
 [12,13,36]

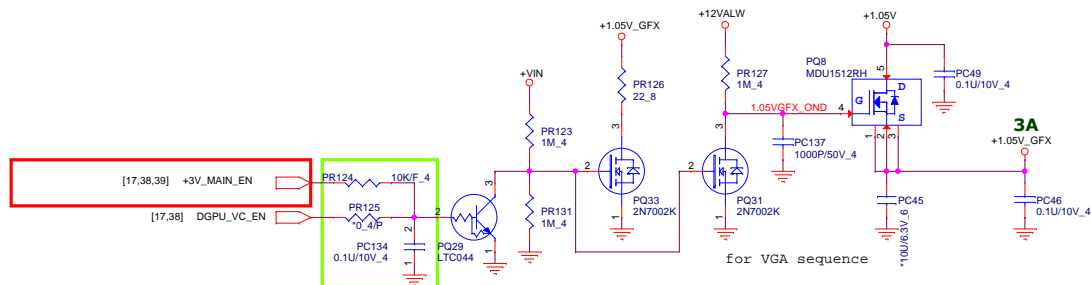
+3V
 +5V
 +VIN
 +3V5S
 +3V5
 +12VALW
 +3VLANVCC
 +0.675V_DDR_VTT

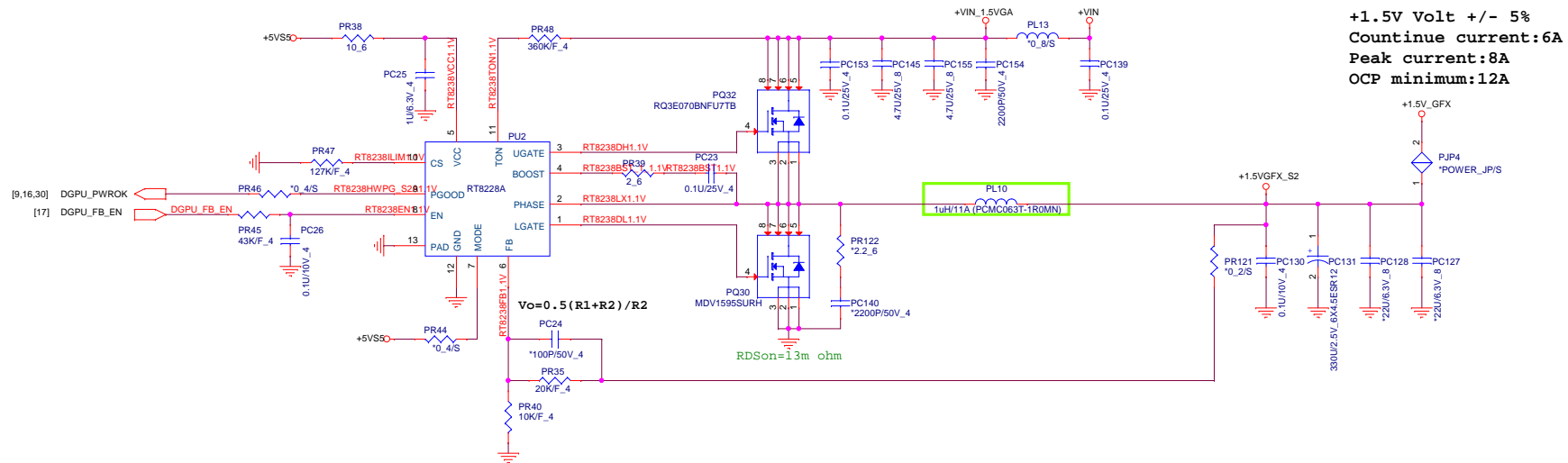


N14P-GS
Countinue current: 35A
Peak current: 55A
OCP minimum 66A

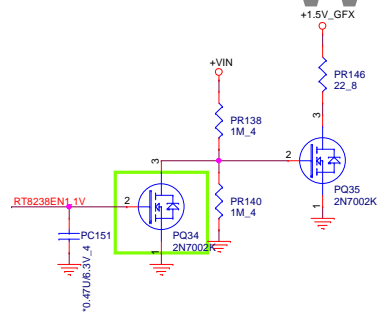


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USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT3	NC	N/A
PORT4	NC	N/A

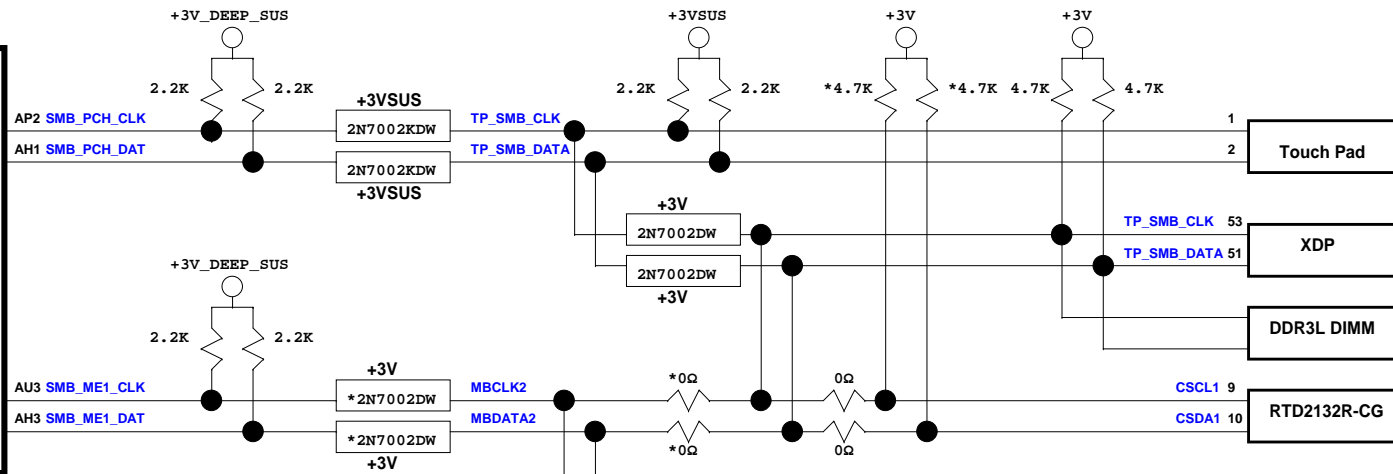
USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON#(from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON(from EC)

SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	mSATA	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

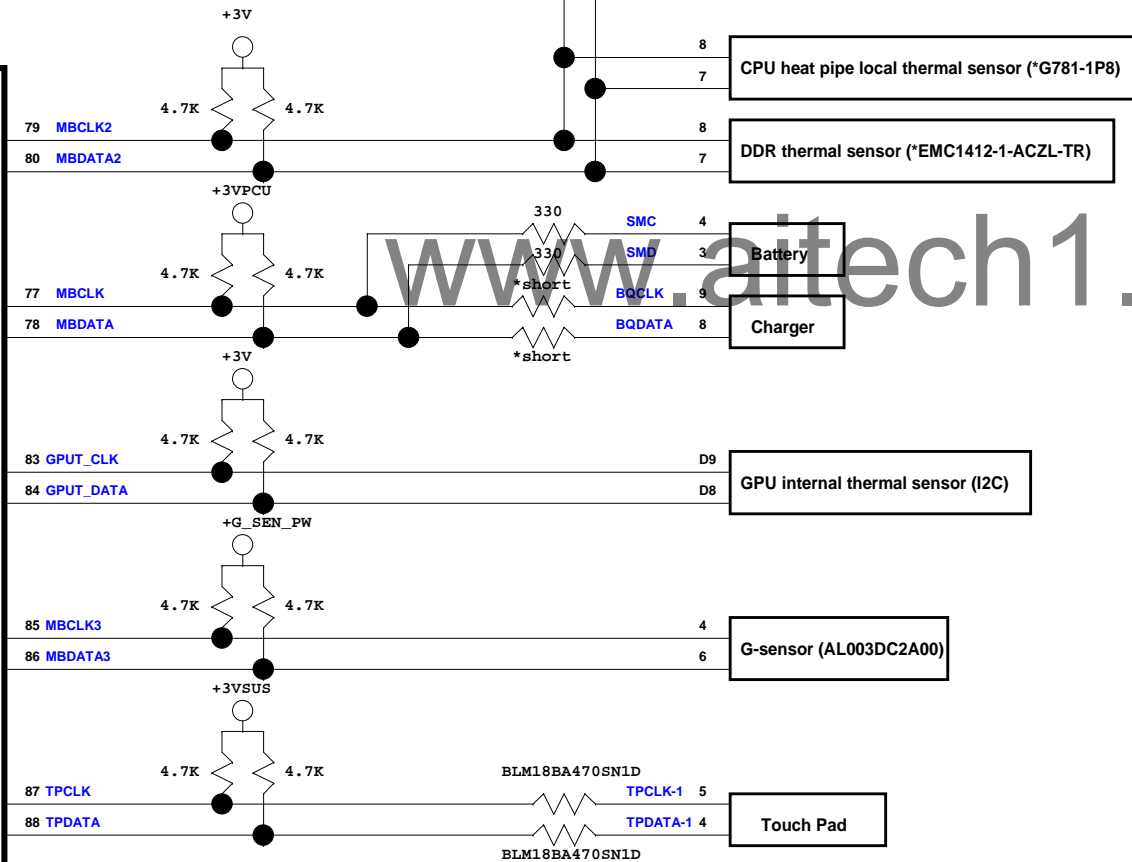
PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	

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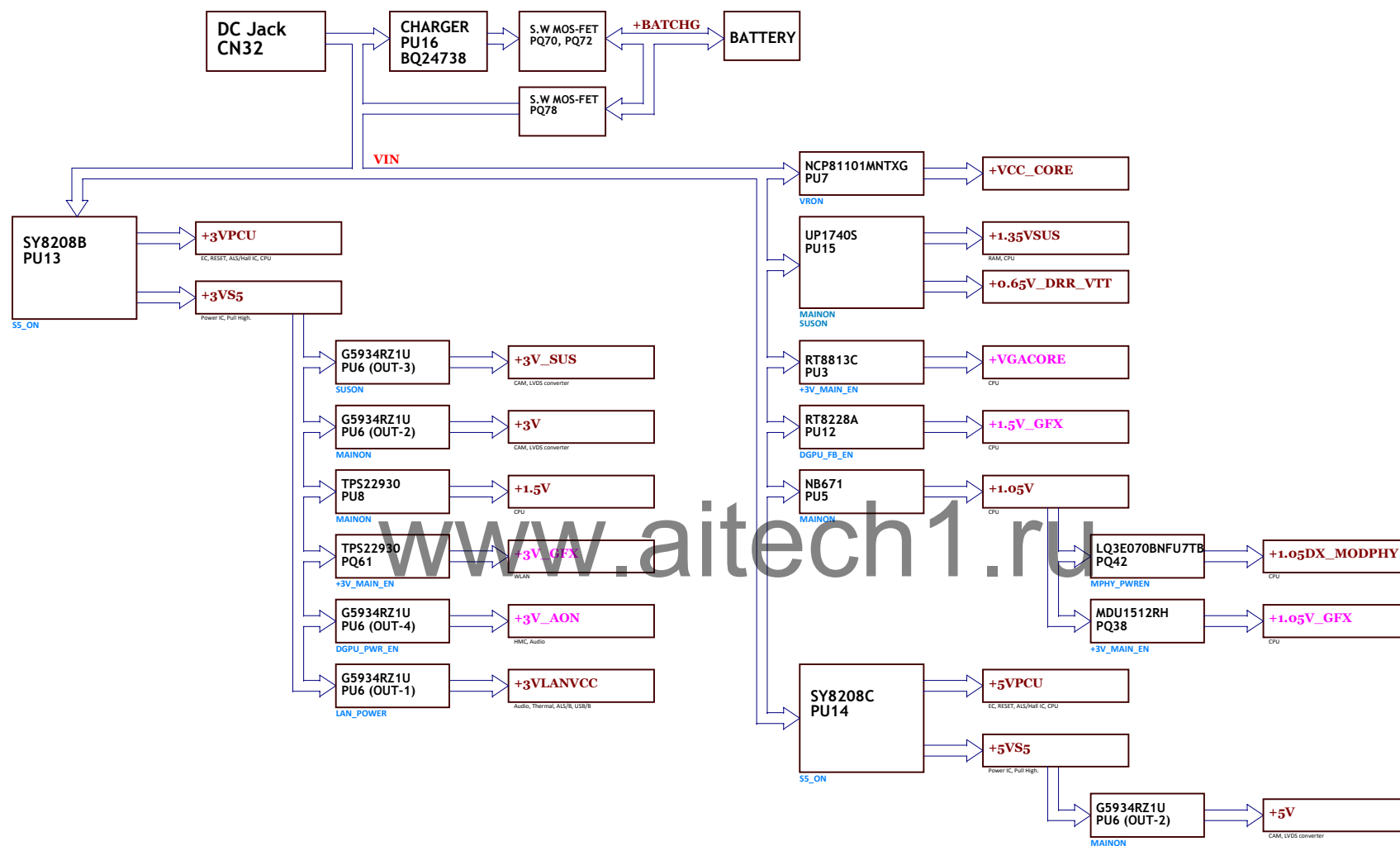
Haswell
ULT

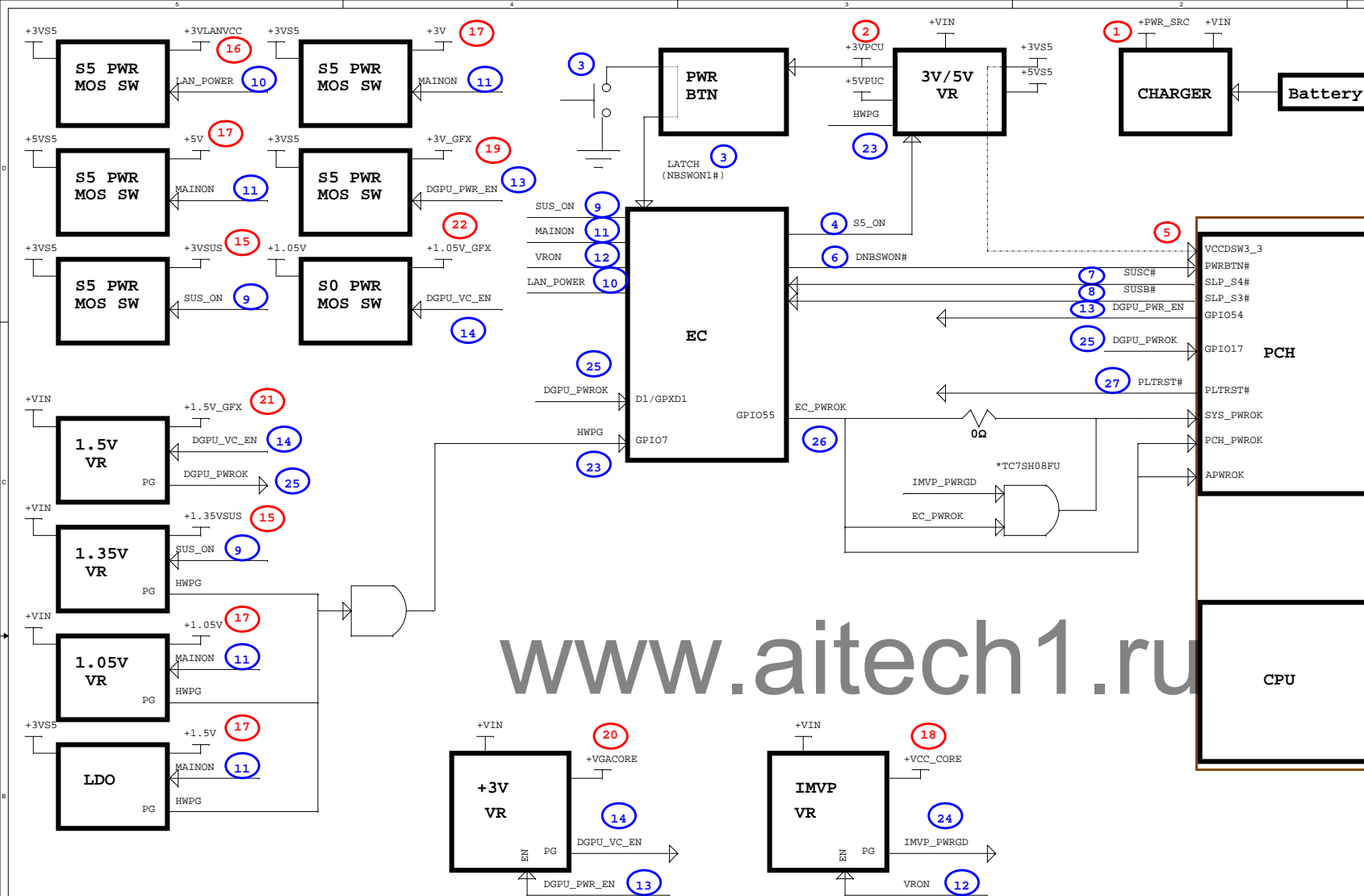


EC
KB9010QF



TWB+JWV SYSTEM POWER BLOCK DIAGRAM





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